

# Uniformity Correlation of AlGaIn/GaN HEMTs grown on 3-inch SiC Substrates

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## I. INTRODUCTION

AlGaIn/GaN HEMT devices are of high commercial and defense interest for microwave amplification purposes because of their ability to provide significantly higher power density and bandwidth compared to conventional GaAs-based HEMTs. For commercial production of the HEMTs, it is very important to obtain a high degree of performance uniformity for the devices fabricated over a 3-inch diameter (larger in future) substrate. At the present state-of-the-art, the non-uniformity of device performance metrics over a full 3" wafer is too high to achieve yield required for commercial realization of the technology. To achieve the high degree of uniformity in device performance, it is essential to understand the source of variation that exists in various structural components of the devices as they are fabricated using standard technology and also the effect of each of these variations on the device performance.

The sources of non-uniformity can come from three levels:

- a) Variation in substrate, which includes crystal quality, surface polish and off-cut angle
- b) Variation in epitaxial growth, which includes crystal quality, uniformity of layer thickness, interfacial roughness, surface roughness, and intentional and unintentional doping uniformity
- c) Variation in device processing, which includes lithography tolerance, tolerance in dry etch, surface damage in dry etch, quality and thickness of deposited metals and dielectrics, quality of the various interfaces between metal, semiconductor and dielectrics, presence of unintentional native oxide layers, various impurity incorporation at different stages of processing, etc.

In addition to understanding the effect of each of these parameters on device performance, it is also important to correlate the tracked parameters between different levels, such as substrate, epi, and device. For example, the effect of substrate surface polish could correlate to surface roughness of the epitaxial layer grown on top. From the list above, it is essential to accumulate and build up a comprehensive database of all the parameters on each level to make meaningful statistical correlations. Given the limitation in resources, parameters that are most expected to have a large effect on performance should be tracked. Following this approach to track and improve uniformity, we have established a systematic data accumulation program, and by

analyzing the data, we have been able to identify certain relationships between these parameters. We summarize some of these results in this paper.

## II. METHODOLOGY

### A. Pre-fabrication

For the present work, the substrates are obtained from various vendors and the epitaxial growth was performed by IQE RF using a Veeco rotating disk reactor. After receiving the as-grown wafers, we perform a comprehensive set of material analysis to understand the variation in substrate and epitaxial layer parameters. The measurements performed are X-ray diffractometry, glancing incidence X-ray reflectance measurement, atomic force microscopy (AFM), optical interference profilometry (Veeco Wyko tool), mercury probe C-V measurement, optical polariscopy, contactless sheet resistivity measurement, and thickness map.

### B. Process control monitors

The HEMT devices were fabricated from MOCVD-grown epitaxial layers on 3" c-plane 6H and 4H Si-SiC substrates. The devices were isolated using RIE etching, and the ohmic contacts were formed with alloyed Ti/Al-based metals. The gate length was defined by RIE etching of SiN<sub>x</sub>, followed by an e-beam lift-off process for the gate metal. All of the standard process control monitors for compound semiconductor processes were collected for each GaN on SiC 3" wafer in a database. Critical parameters such as source, drain and gate CDs, etch rates, over-etch time, and passivation conditions were tracked also. The processing trends will not be discussed in this paper.

### C. Device characterization

After fabrication, the wafers were measured with a set of standard characterization to study the device performance and variation in uniformity. It includes wafer map testing of every site of DC, pulsed IV, and load-pull measurements. S-parameter data is taken on two devices per wafer. An additional set of reliability data is taken per wafer, but will not be included in the present discussion. The DC transfer characteristics are measured at  $V_{DS} = 10V$  and  $V_{GS} = -7V$  to 1.5V. The two-terminal Schottky forward turn-on voltage and reverse breakdown voltage are determined at where  $I_{GD} = 1$  mA/mm. The pulsed IV data are measured by taking two pulsed I-V sweeps. The first  $I_{DS}-V_{DS}$  curve is measured

from  $V_{DS} = 0V$  to  $30V$  at  $V_{GS} = 0V$ , pulsing from a quiescent bias of  $V_{DS} = 0V$  and  $V_{GS} = 0V$ . The second  $I_{DS}$ - $V_{DS}$  curve is measured from  $V_{DS} = 0V$  to  $30V$  at  $V_{GS} = 0V$ , pulsing from a quiescent bias of  $V_{DS} = 30V$  and  $V_{GS} = -5V$ . From these two curves, we have defined and extracted four figures of merit to compare current collapse. The ratio of the 2<sup>nd</sup>  $I_{DS}$  curve, pulsing from  $V_{DS} = 30V$  and  $V_{GS} = -5V$ , to the 1<sup>st</sup>  $I_{DS}$  curve, pulsing from  $V_{DS} = 0V$  and  $V_{GS} = 0V$ , measured at  $V_{DS} = 5V$ ,  $10V$ , and  $15V$  are defined as current collapse figures of merit F5, F10, and F15. We also take the ratio of the area of 2<sup>nd</sup>  $I_{DS}$  curve to the 1<sup>st</sup>  $I_{DS}$  curve as well. All four figures of merit are tracked for each wafer that we complete. For load-pull wafer map testing, the performance was measured at a fixed gate bias and at  $30V$  of drain bias. A reference device was tuned on each wafer and the same impedance was used to carry out the wafer mapping. More than 40 parameters are extracted and tracked for performance uniformity.

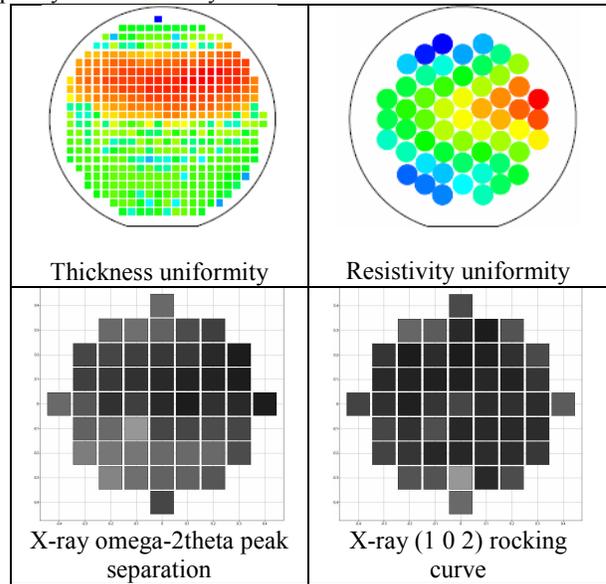
### III. OBSERVATIONS

Analysis of the accumulated data reveals several interesting trends. Data obtained from X-ray rocking curve analysis over 13 points spanning the wafer area indicates that for all vendors, the material quality varies significantly over the whole area of the 3" diameter substrate. Generally, the center area of the wafer is found to have better material quality as well as lesser inclusion of other phases as evidenced by multiple peaks. In addition to crystalline quality, the rocking curve data indicated that the precision of off-cut angle for the substrate also has a large variation. Off-cut angle was found to vary from 0 to as much as 0.5. While statistical data from one vendor indicates that off-cut angle should be less than 0.3 degrees for 83.5% of the wafer, this is still a large variation. In addition to the off-cut angle, wafers are also seen to have a lattice curvature whereby the angle between the crystalline c-plane and the wafer surface vary over the wafer. The variation of this angle over one wafer was found to be as high as 1 degree in some substrates. The off-cut angle and lattice curvature affect the microscopic and macroscopic surface roughness as elaborated later.

Optical profilometry data on 13 points over each wafer were sorted for presence of scratches arising from substrate polish. The data shows that on wafers received in the last 6 months, out of 544 points measured, 23 had scratches of various degrees. While this is a large improvement from the past, the data indicates that surface polish still remains an important issue for the technology. We did not find the scratches being more prevalent over some area of the wafer vs. another.

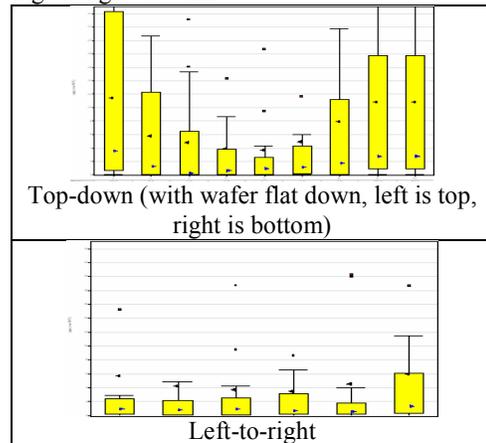
For the epitaxial growth configuration used here, the wafers sit on a platter rotating perpendicular to the gas flow from the showerhead. The centers of all wafers in a specific growth run lie on a circle concentric with the rotating platter with wafer flat lying towards the edge of the platter. If we discount the effect of the spatial variation in the substrate and also some other local issues, the rotation of the platter is expected to cause all points on the wafer that lie at the same radius with respect to the platter to have similar material

properties. For the variation of layer thickness, AlGaN alloy composition (measured by X-ray omega-2theta peak separation) and sheet resistivity, the variation profile is seen to reflect this. This is elaborated in Figure 1. However, the map of (1 0 2) full-width at half maxima (FWHM) does not reflect the symmetry. This is presumably because the substrate crystalline quality has a large effect on the crystal quality of the GaN layer.



**Figure 1. Uniformity map of various parameters for a typical HEMT wafer.**

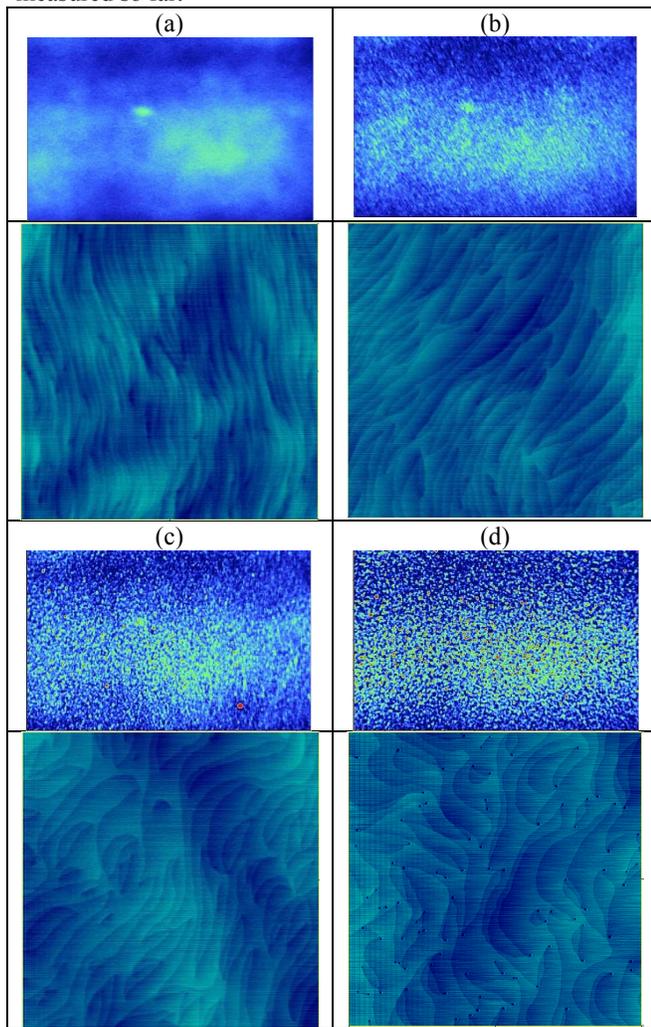
Figure 2 shows the gate current measured under small-signal RF drive ( $I_{GS}$ ) as a function of location on the wafers. A strong top-down dependence was observed, with major flat down. There was almost no lateral variation of  $I_{GS}$  across the wafer. This dependence is strongly indicative of growth-related variation arising from platter-rotation. Even though there is a strong spatial dependence on epi growth, the large variation in device gate current is still dependent on processing changes as well.



**Figure 2. Gate current under small-signal RF drive ( $I_{GS}$ ) variation as a function of position on the wafers.**

As mentioned above, another source of non-uniformity comes from the variation in off-cut angle and lattice curvature in the

SiC substrate. These parameters were found to affect both microscopic (AFM) and macroscopic (Wyko) surface roughness directly. We found that if the local off-cut angle (angle between crystal c-plane and the surface at a given point) is large, then AFM gives a high RMS roughness and the step-flow pattern is seen to be dense, highly directional, and directed perpendicular to the direction of off-cut. If the local off-cut angle is low, then the RMS roughness is small and the step-flow pattern is non-directional and widely spaced. For the macroscopic roughness (Wyko) on the other hand, a small off-cut angle is seen to give a rough morphology with hexagonal hillocks. AFM and Wyko images at points of various off-cut angle are shown in Figure 3. This correlation is found to be true at all data points measured so far.



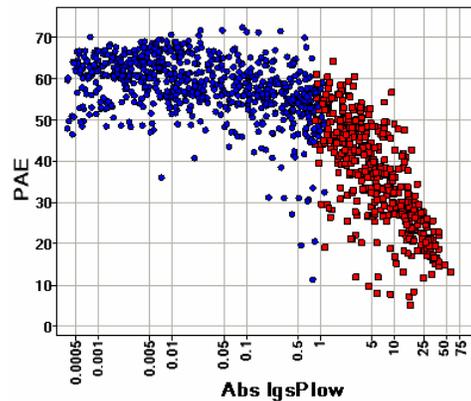
**Figure 3. Progression of micro and macroscopic surface morphology as local off-cut angle is varied from high (about 0.4 degree) from (a) (about 0 degree) from (d) . Top row shows 4.7mm×3mm Wyko image and bottom row shows 5μm×5μm AFM image.**

This behavior seems to be the result of step-flow growth mode similar to the behavior commonly seen for epitaxial growth of GaAs.[1][2]. However, a good correlation between

the various surface morphologies to device performance has so far not been identified.

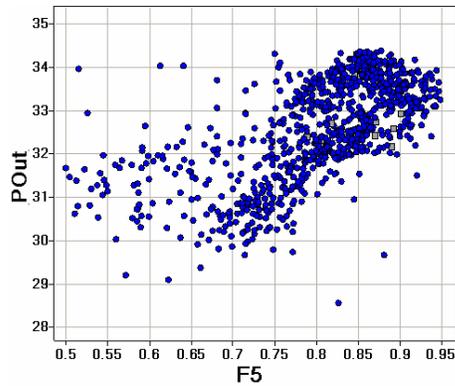
We have also found that C-V measurement can be an effective technique to identify growth variation. Since the C-V data will depend on the layer structure used; only samples of the same layer structure can be compared. We compared the 2V (undepleted) capacitance and conductance measured at 5 points on a diameter going through the major flat for 12 wafers of our standard HEMT structure. The two wafers that showed significantly different behavior at C-V resulted in poor power performance as well. We currently do not understand and are still investigating how C-V correlates with output power.

From our set of standard device characterization, we have observed some general correlations in performance uniformity and yield. Figure 4 shows the peak power-added-efficiency (PAE) as a function of the gate current measured under small-signal RF drive. The results show a strong dependence of PAE on when the gate current is greater than 1 mA/mm. When the gate current is maintained below 1 mA/mm, the correlation of  $I_{GS}$  to PAE becomes less apparent and PAE of greater than 50% can be expected.



**Figure 4. Peak PAE (%) as a function of gate current under small-signal RF drive (mA).**

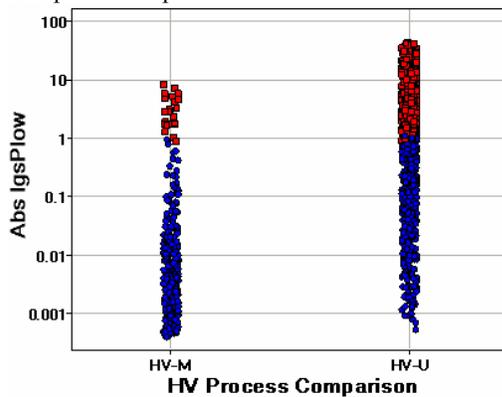
For output power, we have observed a strong correlation to the four current collapse figures of merit. Figure 5 shows the dependence to F5 for 43 GaN HEMT wafers. Since we know that the gate current contributes significantly to variation, only the data points with  $I_{GS} \leq 1$  mA/mm were plotted in Figure 5. In general,  $P_{out}$  increases linearly with respect to F5, however,  $P_{out}$  becomes less dependent on F5 when it's > 0.85.



**Figure 5. Output power at peak PAE (dBm) as a function of current collapse figure of merit at 5V (F5).**

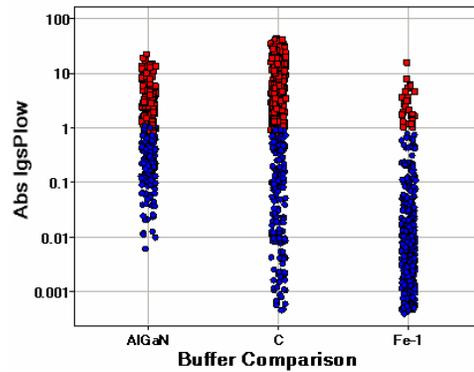
The general correlations shown above of power performance as a function of  $I_{GS}$  and F5 include different process changes and epi structure experiments. To further study the source of non-uniformity in  $I_{GS}$ , thus improving PAE uniformity, we have looked at the dependence of gate current as a function of a process change for the TQNT process and also as a function of GaN buffer and cap thicknesses.

Figure 6 shows gate current variations for wafers fabricated with different processing techniques. The gate structure, passivation, and interconnects were the same, but there were changes in developer and clean-up methods. Clearly, “HV-M” process has consistently produced low gate current, except for a few scattered data points above the threshold of 1 mA/mm. In contrary, “HV-U” process yielded extremely non-uniform result, where there is a large spread in gate current. Therefore, the performance variation that we observe is process-dependent.



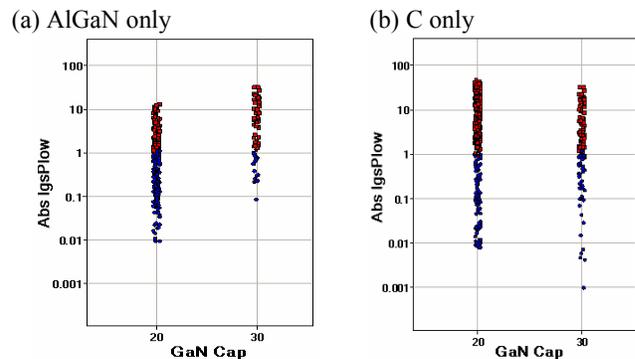
**Figure 6. Gate current under small-signal RF drive (mA) as a function of process differences**

Further looking at the wafers fabricated with “HV-U” process as a function of buffer in Figure 7, we observed that the process becomes much less sensitive to the Fe-doped buffer material. Both C and AlGaN buffer show similar spread. Note that the data includes two GaN thickness variations.



**Figure 7 Gate current variation for three buffer types.**

For the “HV-U” process, the results show that the GaN cap thickness does not seem to improve the gate current uniformity for both types of buffers, as shown in Figure 8.



**Figure 8 (a) Igs vs. GaN cap for AlGaN buffer only, (b) Igs vs. GaN cap for C doped buffers only**

## IV. CONCLUSIONS

In this paper, we have presented our methodology for establishing a system to track variations in substrate, epi quality and device performance. We have also discussed some of our observations in material and device performance. We believe that through the systematic data collection and analysis, we will be able to advance the device uniformity and yield for commercialization of GaN HEMT wafers.

## REFERENCES

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2. M. Shinohara, and N. Inoue, *Appl. Phys. Lett.* **66**, 1936, (1995).