Status of SEMI Standardization Efforts in Compound Semiconductors

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Abstract

The SEMI (Semiconductor Equipment and Materials International) North American Compound Semiconductor Committee is organized into five Task Forces: Indium Phosphide, Indium Antimonide, Gallium Arsenide, Silicon Carbide, and Electrical Properties. Progress and current status of the projects undertaken by the committee and task forces are reviewed and outlined. In addition the cooperative programs between SEMI Standards and ASTM are discussed.

INTRODUCTION

SEMI is a volunteer-driven organization dedicated to the exchange of information among suppliers and users within the semiconductor industry. SEMI Standards [1] provide a global platform to achieve agreement on specifications, procedures, and characteristics for semiconductor materials and equipment. This global consensus ensures compatibility of goods and services and provides a framework for establishing the future direction of the semiconductor industry. The silicon industry has adopted SEMI standards as a way to determine and influence the evolution of industry trends, letting standards and roadmaps lead the industry directions. The compound semiconductor industry (with fewer resources and markets) has been a late adopter, typically defining standards only after the product is on the market place. As a result a consensus is more difficult to achieve often resulting in multiple options or choices for various parameters. This paper will highlight and summarize the current standards development activities of the task forces within the North American SEMI Compound Semiconductor Committee. The intent is to show current and future tasks and to highlight where new standards and industry consensus will benefit the entire compound industry.

SEMI COMPOUND SEMICONDUCTOR ORGANIZATION

SEMI Standards committees [2] are organized regionally in Japan, North America (NA) and Europe for logistical and historical reasons. Representation from all companies is encouraged and all meetings are open to all personal or company participation regardless of official SEMI membership. SEMI Standards committees typically meet two or three times per year to approve and transact formal business. The majority of the detailed specification and document development is completed at the sub-committee level through Task Forces (TF). These Task Forces may function within a region, have regional representation or be truly global, with participation from technologists worldwide. They may be task oriented and disbanded after completion, or function constantly. As an example, GaAs work is accomplished by task forces in each of the separate regions while SiC is a truly global task force with most of the work accomplished through teleconferences and e-mail rather than face-to-face meetings. Despite how the documents are developed and ultimately specifications written, all approval and electronic balloting are carried out on a global basis.

INDIUM PHOSPHIDE TASK FORCE

The Indium Phosphide task force has completed the standard: **SEMI M23 Specification for Polished Monocrystalline Indium Phosphide Wafers** which includes physical characteristics for 50mm, 3-inch, 100mm and 150mm diameter wafers. The most recent task force action was to update the wafer laser marking requirements and adapt the specification to include InP and other compound semiconductors. With the scope and title now changed, the standard **SEMI T5, Specification for Alphanumeric Marking of Round Compound Semiconductor Wafers** includes the laser marking requirements for GaAs, InP, as well as SiC, InSb and other

compound semiconductor substrates. With this work completed, the task force was officially disbanded in November 2006.

INDIUM ANTIMONIDE TASK FORCE

The Indium Antimonide task force held its initial meeting at CS Mantech 2006. At that time InSb wafers were beginning a transition from 3-inch to 100mm diameters which illustrated the need for standardization of some common wafer characteristics. The CS Mantech meeting attracted interest from a number of in-person and phone-in meeting participants. The initial premise of the group was to adopt the specifications of GaAs (or Si) as the basis and only where there is an overwhelmingly compelling reason, choose a different standard value. The task force has concentrated on dimensional and physical characteristics and has chosen to include 3-inch through 100mm diameters in the initial work. Wafer thickness is a prime example where the significantly different density (weight) and brittle nature of InSb require a special consideration in thickness values. Table 1 lists some tentative suggestions for InSb specifications.

TABLE 1.
PROPOSED DIMENSIONAL AND FLATNESS SPECIFICATIONS FOR INSB WAFERS.

InSb Draft Specifications				
	3-inch	**85 mm**	**100 mm**	
Diameter	76.2 +/- 0.5	85 +/-0.5	100 +/-0.5	mm
Orientation	<111>	<111>	<111>	
+/-	0.5°	0.5°	0.5°	degrees
Major Flat	22 +/- 2	32.5 +/-2.5	32.5 +/-2.5	mm
Minor Flat	11 +/- 2	18 +/-2	18 +/-2	mm
Thickness	800/900	1200	1200	µm
+/-	25	25	25	µm
Bow	10	10	10	µm
Warp	10	10	10	µm
TTV	10	10	10	µm

GALLIUM ARSENIDE TASK FORCE

Gallium Arsenide has active task forces in each of the international regions. At the present time there are three standardization activities underway: 200mm Diameter GaAs wafers, 150mm Diameter GaAs wafers, and the "five year" review and re-approval of standards for smaller diameter GaAs wafers.

The 200mm GaAs standard was published last year: **SEMI M9.8 Specification for Round 200mm Polished Monocrystalline Gallium Arsenide Wafers (Notched).** The effort was focused on defining the geometrical parameters for 200mm diameter wafers. There were two main areas of discussion: wafer thickness and position of the laser marking. In the diameter transition of silicon from 150mm to 200mm, specifications also increased the wafer thickness from 675um to 750um. Due to the higher density of GaAs, ergonomic considerations of cassette and wafer weight prompted a theoretical study to see if a similar increase in thickness was necessary. The study showed no reason to expect increased breakage, and as a result the wafer thickness was maintained at 675um.

Larger diameter GaAs wafers, 200mm (and 150mm) have a notch for orientation identification instead of flats. While the SEMI standard position for the laser identification marking on 150mm wafers is adjacent to the notch, for 200mm wafers, two position options are offered. One is adjacent to the notch, the second position is rotated 45 degrees clockwise (CW) from the notch. [1] This position interferes less with patterning and offers some advantages during dicing operations.

For 150mm GaAs wafers there are two main areas of discussion in the revision of the document **SEMI M9.7 Specification for Round 150mm Polished Monocrystalline Gallium Arsenide wafers (Notched)**: position of the laser mark, and wafer flatness parameters. As mentioned previously, the current standard has the laser mark adjacent to the notch, and consideration is given to also specifying the location 45 degrees CW from the notch, as an option. In addition there is lack of consensus on whether the mark should be on the process (front) or back side of the wafer, although the current SEMI standard location is the front side. The second major issue is the particular wafer flatness and shape measurement parameters to be used in the specifications. Large diameter silicon specifications utilize specialized global and site flatness parameters [3] (for example, GP3D and SFQR) and shape parameters (for example, GFLYFER and GB3MMPR). Compound semiconductor operations have typically used similar parameters for flatness [4] (for example, TTV and LFPD) and shape (bow and warp) that are simpler to measure.

All SEMI Standards are required to be reviewed and re-approved on a five year basis. This has been low priority and sorely neglected in the recent past. The SEMI Japan GaAs Task Force is undertaking a review of the GaAs wafer specifications, and has recently balloted the specifications for 2-inch, 3-inch 100mm and 125mm diameter GaAs wafers without change from the previously approved documents.

[1] Note that this is where the major flat (V-Groove option) would be if these wafers had flats.

SILICON CARBIDE TASK FORCE

Silicon carbide is organized into a global task force led through the European Compound Semiconductor committee, but with representation from committees in North America and Japan, and with participants from throughout the world. Over the last couple years this SiC global task force completed documentation of physical dimensions and flatness parameters for SiC wafers: **SEMI M55- Specification for Polished Monocrystalline Silicon Carbide Wafers**. Specifications for 2-inch and 3-inch wafers are included, but 100mm wafer parameters are still in draft form (draft document 3874). The particular values for wafer thickness and tolerance, flatness parameters, and off-orientation are still not resolved. Some of the current suggested specifications are listed in Table 2. Note the large number of possible combinations using the proposed options. Merging potential thickness and orientation options creates an exceptionally large number of "standard" product variations. This reflects the completely different substrate requirements for optical, microwave RF and high voltage power devices. Further standardization would reduce the variety of possible options. This example highlights the need and benefit from adopting a 100mm SiC wafer standard.

TABLE 2.
PROPOSED SPECIFICATIONS FOR 100MM SIC WAFERS.

	100mm SiC Wafers Range of Proposed Specifications	
Diameter	100 +/-0.25 mm	
Primary Flat Length	32.5 +/-2.0 mm	
Secondary Flat Length	18.0 +/- 2.0 mm	
Thickness	450 +/-25 µm	
	400 +/-25 µm	
	350 +/-25 µm	
Bow	+/- 25 µm	+/- 40 µm
Warp	<25 µm	<40 µm
TTV	<20 µm	<25 µm
Wafer Orientation or Off Orientation	0 + 0.25 deg	
	4 +/-0.5 deg toward <1-100> direction	
	8 +/- 0.5 deg towards <1-100> direction	
	4 +/- 0.5 deg towards <11-20> direction	
	8 +/- 0.5 deg towards <11-20> direction	
Maximum Defect area	10%	30%
Edge Exclusion	3 mm	

The North American task force has undertaken additional activities. Currently a resistivity measurement working group is examining test methods and specifications for measurement of resistivity on semi-insulating (SI) SiC. A pilot study sample exchange between various vendors and measurement laboratories is underway with the intent of establishing a standard which includes test methodology and SI-SiC specifications. The study includes three US SiC vendors who have supplied SiC wafers. In addition to the vendors, measurements will also be made by three equipment vendors and one US government laboratory (Air Force Research Laboratory). AFRL will act as the data collection and analysis coordinator to evaluate the differences in contact, non-contact, and destructive measurements.

Future task force work is currently under consideration. SiC wafers are used for a variety of devices (GaN LED, high voltage switch, RF etc.) which have conflicting substrate requirements. A survey is underway to determine the industries suggestions and requirements for future standards documents.

ELECTRICAL PROPERTIES TASK FORCE

The electrical properties task force combines its work with ASTM International to develop test methods applicable to compound semiconductors. Primary work of the task force has been in two areas: resistivity and mobility measurements. Currently the resistivity standards available from NIST and NIST traceable laboratories are certified only for the center measurement. With the industry emphasis on improved wafer uniformity, there is a strong interest in standards and methods to quantify the within-wafer resistivity variability or deviation. In addition there are subtle differences in instrument calibration when the samples are bulk silicon, versus epitaxial layers on semi-insulating GaAs. The task force proposes a sample exchange to compare measurements using four-point probe, destructive Hall, non-contact Hall, and eddy current resistivity measurements to evaluate the resistivity measurement techniques.

In addition, a round-robin sample exchange for mobility measurement is in progress. Four different pHEMT wafers with 5 samples from each wafer (sizes 10x10mm and 40x40mm) have been measured at about a dozen different tests facilities using contact Hall measurements and non-destructive RF power absorption/reflection measurements. Data analysis is currently underway to separate the effects of pHEMT cap layer thickness on the 2DEG mobility as well as variability between the different techniques and laboratories.

ASTM – SIC MICROPIPE COUNTING

SiC micropipe counting [5] is an ASTM project (WK5615) that is assisted by the SEMI SiC task force. A round robin experiment was conducted to compare the precision and accuracy of the current state of the art in micropipe

counting on SiC wafers. Thirty semi-insulating, conducting, and n+ samples were exchanged among nine SiC wafer suppliers and users. Samples were measured using the laboratories standard counting technique as well as x-ray topography. Laboratories utilizing non-destructive techniques measured most of the samples while those labs using a destructive technique measured "adjacent wafers" one from each of the five ingots. Variability among the different techniques exceeded a factor of three in micropipes counted. Attempts were made to prescribe the areas to be counted and to sort out the effects of mistaken counts for micropipe clustering. Further analysis of the multi-laboratory data is underway.

ASTM - TEST METHODS DEVELOPMENT

Test methods or procedures may be developed and published within SEMI but also are developed within the ASTM organization. Over the last year SEMI has completed the acceptance and transition of the "silicon specific" ASTM test methods and merged them into the SEMI standards. The ASTM documents are now available, and revised through the SEMI Standards organization. They are included in the Materials and Process Control section of SEMI and are renumbered with an M prefix to the original ASTM designation. The ASTM standards relating to compound semiconductors (e.g. **ASTM F76-Standard Test Methods for Measuring Resistivity and Hall Coefficient …**) are still under the auspices of ASTM committee F01.15 and have not been transferred to SEMI.

SUMMARY

The SEMI Compound Semiconductor Materials Committee is organized globally with task forces in each of the three active regions participating in the world-wide standards development process. A description of the standards documents and activities of the Compound Semiconductor Committee recently completed and under development is presented.

Requests for additional information, suggestions of standards activities, or enrollment in committees may be accomplished through the SEMI website (www.semi.org), or by contacting the authors or a SEMI staff member [6].

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REFERENCES

[1] Weiss, B. "The SEMI International Standards Program: History, Successes and Lessons Learned to Address Compound Semiconductor Manufacturing Challenges" Digest of 2006 Compound Semiconductor Mantech Conference, Vancouver BC pg. 55-58

[2] Oliver, J. D., Kremer, R. "SEMI Standardization Efforts in Compound Semiconductors" Digest of 2006 Compound Semiconductor Mantech Conference, Vancouver BC pg. 265-268

[3] SEMI M1- Specifications for Polished Monocrystalline Silicon Wafers, www.semi.org

[4] SEMI M9- Specifications for Polished Monocrystalline Gallium Arsenide Wafers, www.semi.org

[5] Emorhokpor, E. et. al. "Comparison Between Measurement Techniques Used for Determination of Micropipe Density in SiC Substrates", 2005 International Conference on SiC and Related Materials Pittsburgh PA, Materials Science Forum Vols. 527-529 (2006) pp 443-446

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