Yield Enhancement of 0.15um pHEMT Milli-meter Wave Power Amplifiers using an Effective Statistical Analytical Approach

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Abstract

WIN's 0.15um power pHEMT technology has been popularly used by customers to design and produce Ka- to V-band power amplifier MMICs. It is a robust production technology that produces high performance and high yield PA products. The functional yield is usually high; average Ion/off and breakdown voltage yield are over 75% even for the output power of 4-6W at Ka-band with total gate periphery over 10mm. However, in one particular case, one of the milli-meter-wave high power PA circuits was characterized by relatively low circuit yield. This was attributed to a requirement of more stringent circuit specification of DC/RF characteristics for this special circuit. To improve the circuit yield, both epitaxial structure and wafer process require a more precise and better control. At WIN, we have statistically analyzed and correlated the data among circuits, epitaxial material and process. With very concise and elaborate statistical data analysis and physical understanding on all parameters, including circuits, epitaxial material and process, we have made a significant improvement of circuit yield. In this paper, we will present our statistical analytical approach and data analysis that leads to a significant improvement of a 0.15um high power pHEMT circuit yield.

INTRODUCTION

In semiconductor manufacturing, yield is always one of the most important factors for consideration. It critically determines the profit margin in the company. The improved yield can lead to the growth of profit while the deteriorated yield loss can result in the increase of loss. In order to maintain a high yield process or continue to improve yield, we should constantly monitor the yield, analyze the yield loss factor(s), perform the root cause search and implement the corrective actions on the major defects.

In this paper, we present a methodology of how we analyzed the wafer level screening data and compare it to the PCM (process control monitor) parameters to find out the possible failure modes. As a result, we are able to improve the yield effectively.

METHODOLOGY

WIN's 0.15um power pHEMT technology has been popularly used by customers to design and produce Ka- to V-band power amplifier MMICs[1]. Figure1 shows the major process flow for our current pHEMT technology. When the wafers completed, the wafer-level screening test including the DC and RF characterization would be performed; the KGD (Known Good Die) could then be identified and determined. In order to improve the wafer-level screening yield, the possible failure mode analysis on the test data would be the first and also the most important step. We used the statistical methodology like histogram, box plot, etc to figure out what the possible causes of the chips failure are and then we could generate a defect Pareto to prioritize the improvement activities to speed up the yield improvement.

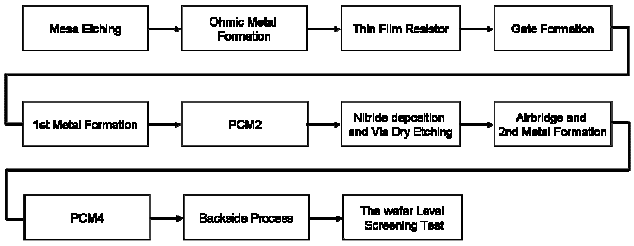

Figure 1. Process Flowchart of WIN 0.15um power pHEMT

Besides, at WIN, we screen the fabricated wafers with PCM (Process Control Monitor) in-process testing at the several critical process steps. We collected the PCM data and sort out the most important parameters from them. The selected PCM parameters were then compared with the screening data to investigate if there is any correlation between the PCM parameters and the screening data. In addition, to get a timely warning on low screening yield and to reflect the screening yield of real circuit, we also studied to find bias condition and spec on a specific simple PCM

device. Finally, a set of criteria was applied to the PCM testing method in order to obtain possible failure modes.

When the screening data and PCM data were anatomized, in the ideal case, the possible failure modes should be able to be categorized easily into either process-related or epitaxial material-related, but in practice, the failure modes are often in the mixture of both and need to be investigated carefully.

ANALYSIS AND RESULT

The wafer level screening yield improvement process consists of four parts: (1) screening data analysis, (2) PCM data analysis, (3) a better control of the epitaxial material, and (4) manufacturing process improvement.

1. Screening data analysis:

In the wafer-level screening test, there are mainly two DC measurement items being performed, Ion/off and breakdown voltage test. The test conditions for these two DC measurements are showed as the table I.

Table I. The test condition of breakdown test and Ion/off test

Screening Test Item	Test Condition
Breakdown Voltage Test	Vgs=-5V, Vds=5V, measure Id
Ion/off	Ion: Vgs=-2.5V, Vds= 3V, measure Id
	Ioff: Vgs=-1.3V, Vds= 3V, measure Id

From the screening test data, the preliminary statistical analysis shows that the most dominant factor of the yield loss was due to the breakdown voltage test failure (Fig.2). In addition, we analyzed the yield distribution for breakdown screening and found multiple peaks in the yield distribution as shown in figure 3. It suggests that there should be multiple failure modes in the breakdown-screening test.

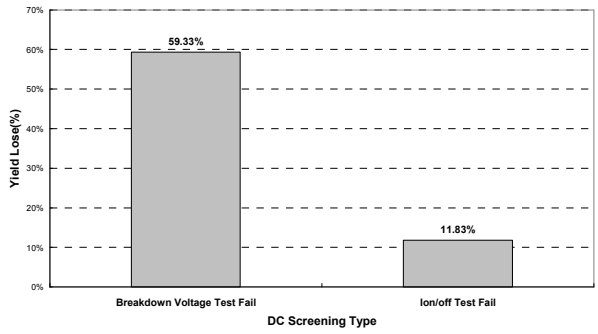

Figure 2. The yield loss of the two DC screening parameters

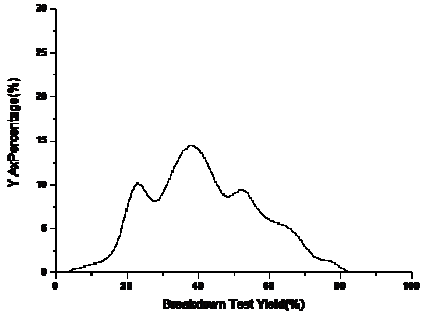

Figure 3. Breakdown test yield distribution

After further investigation on the breakdown screening data, we found that the majority of the failed chips have pretty high leakage current (Fig.4). This indicates that the devices cannot pinch off very well under the breakdown test conditions. There should be several mechanisms to account for this behavior. The first possibility is due to the poor gate quality, for example, the gates broken or slightly detached from the recess area, etc. This could increase the leakage current significantly when applied the breakdown test condition. Secondly, the epitaxial material would be another factor to cause the devices not to survive under the breakdown test since the intrinsic breakdown is not high enough.

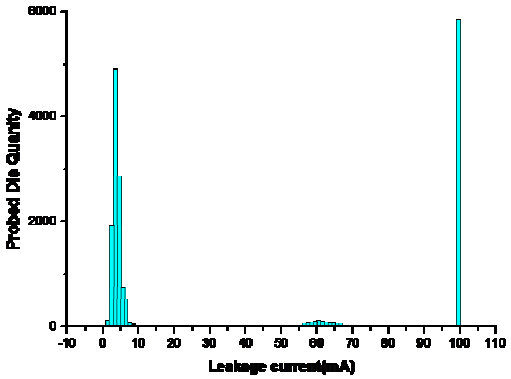

Figure 4. The histogram of leakage current at the breakdown-screening test

2. PCM data analysis

Since the analysis result from wafer screening data shows that the breakdown voltage is the main yield killer and the failure modes could be related to both the epitaxial material and gate quality, the next step was to study whether there are any PCM4 (measured after front side completion) parameters that could predict the breakdown voltage screening results in advance when wafer is still in the process, before the final wafer level screening test stage. After extensive studies, we found that there were two PCM4

parameters, VDG (breakdown voltage) and IPO (3-termianl leakage current) that have high correlation to the breakdown screening yield. VDG is the breakdown voltage between drain and gate when Ig reaches 1mA/mm and IPO is the leakage drain current at Vgs of -2V and Vds of 1.5V.

These PCM4 parameters are measured on a 1-gate finger device with 75um gate width. Figure 5 and 6 show that wafers were separated into three groups with different VDG and IPO average values. The group with higher VDG and lower IPO values showed a lower breakdown screening yield loss. This suggests that if the intrinsic VDG is increased or IPO is decreased, the impact on breakdown screening yield would be decreased. Theoretically speaking, these two PCM4 parameters are mainly dominated either by the Epitaxial material or the processes. Therefore, to get a better control on Epitaxial material definitely became an important item on the yield improvement.

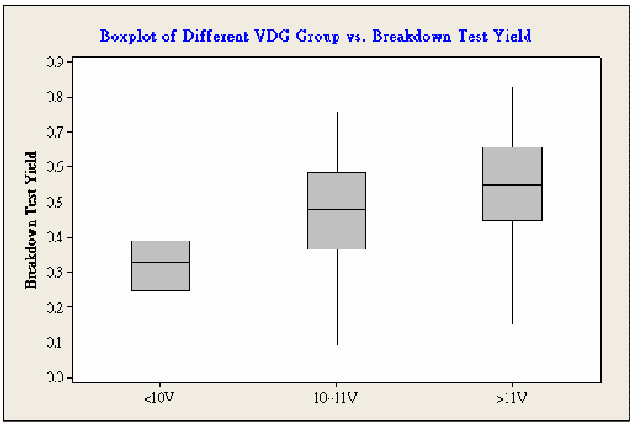

Figure 5. Higher PCM4 Breakdown voltage (VDG) corresponds to lower breakdown screening yield. The PCM4 breakdown voltage was defined as Ids at 1mA/mm measured on a device of 1gate finger with 75um gate width.

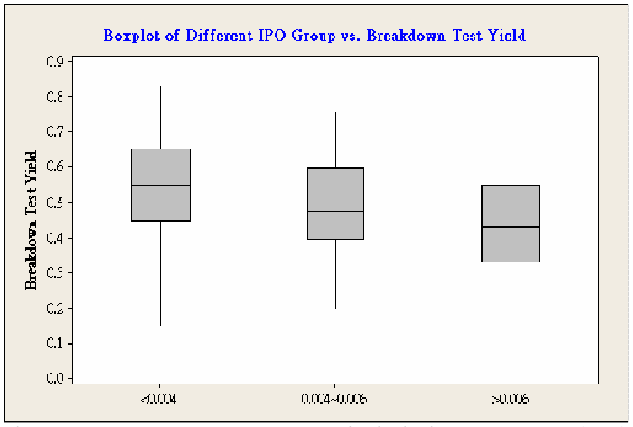

Figure 6. Lower PCM 3-terminal leakage current (IPO) corresponds to lower breakdown screening yield. The PCM 3-termial leakage current was measured on a device of 1gate finger with 75um gate width at Vgs=-2V and Vds=1.5V.

From figures 5 and 6, we also observed a very wide distribution for all three groups on the breakdown voltage test screening yield loss. This means that the process variation would also influence the breakdown voltage screening test yield in addition to the better Epitaxial material control.

3. Epitaxial material better control:

From the screening data analysis, we knew that the control of Epitaxial material could play a very important role on PCM4 VDG and IPO, and thus affect the breakdown-screening yield. But how do we know if the Epitaxial material has good intrinsic VGD? We asked our Epitaxial grower to grow the epitaxial material with different PCM2 VDG values. The PCM2 is measured right after 1st metal formation and would have a better indication of the Epitaxial quality. These wafers with various Epitaxial conditions were processed and sent to the screening test. Figure 7 shows that if the wafers have higher breakdown voltage, the DC screening test yield would also be increased. However, the change in Epitaxial conditions to increase VDG would also cause the current as well as the power and current gain to drop. Therefore, we could not increase the VDG in order to get the best breakdown screening yield, but need to take the impact of RF performance into consideration.

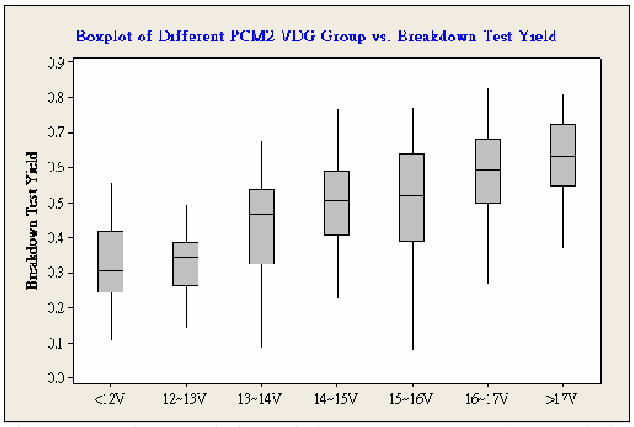

Figure 7. The correlation of the PCM2 VDG values and the breakdown screening yield distribution.

4. Process improvement:

The gate formation process as usual is the major player of 0.15um pHEMT yield. The breakdown-screening test is a 3-terminal leakage current measurement on the MMIC, although the intrinsic breakdown voltage is high, if the gate is not healthy, the leakage current would be high so that the breakdown screening test would fail. This could explain the large variations (ranges) in figure 5. The majority of the failed chips on wafers with high breakdown screening yield are probably due to pretty high leakage current. The Epitaxial material should be not play a role here since these

wafers have good intrinsic VDG and IPO. The distribution of the leakage current on almost all the failed chips was found to reach 100mA. This indicated that the gate would be broken or damaged, so when the breakdown voltage was applied on the MMIC, the device could not pinch-off or the gate was burned-out. In order to get the good quality gate, we have a set of process improvement activities on gate formation, including the gate photo resistor thickness tuning, recess etching solution and etching time tuning, gate metal lift-off process optimization, etc.

After the gate process improvement been implemented together with a better control on the Epitaxial material, the breakdown voltage test-screening yield had a significant improvement from 40% to 60% as shown in figure 8. Figure 9 shows that the center of the distribution moves toward the high yield direction after improvement.

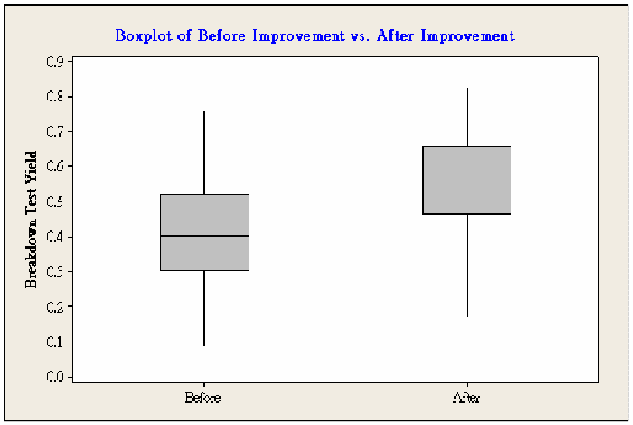

Figure 8. Breakdown yield comparison before and after the process and epitaxial material improvement

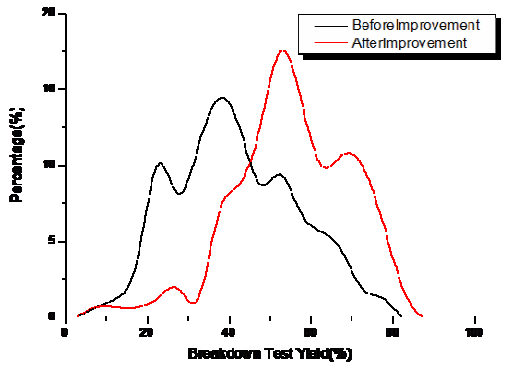

Figure 9. The yield distributions before and after improvement

CONCLUSIONS

We have shown an effective approach to extract the defect Pareto from the wafer level screening data and correlate the test yield with the PCM data. The methodology and analysis results could be used to prioritize the yield improvement activities. The key idea of this methodology is to use the wafer level screening data to observe the main failure modes and then provide the corresponding solution or improvement in the process line. A significant improvement in the final test yield with a tighter distribution was achieved.

REFERENCES

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