Enhancement-mode metamorphic InAlAs/InGaAs HEMTs on GaAs substrates with reduced leakage current by CF_4 plasma treatment

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Abstract

Enhancement-mode metamorphic InAlAs/InGaAs HEMTs grown by MOCVD on GaAs substrates have been fabricated using CF_4 plasma treatment. Shifting of the threshold voltage from negative (depletion mode) to zero (enhancement mode) can be adjusted with process parameters. The plasma process provides a side benefit of reducing the leakage current of the device up to two orders of magnitudes. Depletion-mode and enhancement-mode devices fabricated from the same epi-wafer are compared, both with reasonably good device performance. Transistors with 1.5μm gate length exhibited transconductance up to 315mS/mm and current gain cut off frequency (f_T) of 17.9GHz and maximum available gain (f_{max}) of 80GHz. Confirmed by atomic force microscope (AFM) measurements, thickness reduction of the InAlAs layer treated by CF_4 Plasma is less than 1nm.

INTRODUCTION

Direct-coupled FET logic (DCFL) by integration of enhancement/depletion-mode (E/D-mode) HEMTs offers a simple circuit configuration that is critical for high speed and high-density digital circuit applications. Compared to lattice-matched AlGaAs/GaAs and AlGaAs/InGaAs PHEMTs, InAlAs/InGaAs MHEMTs provide higher two-dimensional electron gas mobility and carrier drift velocity. Therefore, it is a promising technology for the realization of ultrahigh-speed circuits. Several ways, such as the two-step gate recess etching and the buried gate technology (e.g. Pt [1], Ir [2]), were used to achieve E/D-mode devices on the same epi-wafer. However, the two-step gate recess etching approach requires special design of the epitaxial structure, which required the growth of E-mode and D-mode barrier layers respectively. Also, it is very difficult to choose the right chemical solutions to etch the E/D-mode gate recess selectively. The gate metal sinking process also requires a gate-recess step that modifies the pinch-off voltage to a value close to zero volt. Here, we demonstrated a technique to fabricate E/D-mode InAlAs/InGaAs MHEMTs using a fluoride-based plasma treatment process [3]. This technology not only realized E/D-mode devices on the same chip, but also reduced the leakage current up to two orders of magnitude. In the past, high buffer leakage current of MHEMTs grown by MOCVD plagued its performance. Therefore, reduction of the leakage current is a significant improvement of the metamorphic technology by MOCVD.

DEVICE FABRICATION

Metamorphic $In_{0.51}Al_{0.49}As/In_{0.53}Ga_{0.47}As$ HEMTs lattice-matched to InP were grown on 4-inch (001) oriented semi-insulating GaAs substrates using an Aixtron AIX-200/4 MOCVD system [4]. Table 1 is the epitaxial structure of the MHEMTs. Room temperature Hall mobility of 2DEG is over 7000cm^2/V-s with sheet carrier densities larger than 4.8E+12cm^2.

Table 1
Schematic of MHEMTs structure grown on GaAs

Si-doped $In_{0.53}Ga_{0.47}As$ ($n=5x10^{18}cm^{-3}$)	150A	Cap layer
i-$In_{0.51}Al_{0.48}As$	150A	Barrier layer
Si-planar doped	$4x10^{12}cm^{-2}$	
i- $In_{0.51}Al_{0.48}As$	50A	Spacer layer
i- $In_{0.6}Ga_{0.4}As$	270A	Channel _1
i- $In_{0.53}Ga_{0.47}As$	150A	Channel _2
HT- $In_{0.51}Al_{0.48}As$	1000A	Buffer_6
LT- $In_{0.51}Al_{0.48}As$ (linear grade to HT)	2000A	Buffer_5
LT-InP: C	1000A	Buffer_4
HT-InP	6500A	Buffer_3
LT-InP	1100A	Buffer_2
GaAs	1000A	Buffer_1
S.I. GaAs Substrate		

Device mesa was formed by wet chemical etching using H_3PO_4:H_2O_2:H_2O=3.1:50, and then the mesa-sidewall was selectively recessed using citric acid: H_2O_2=1:1 to reduce the gate leakage current. A six-layer metal system (Ni/Ge/Au/Ge/Ni/Au) was evaporated to form ohmic contacts. The non-alloyed ohmic contact resistance Rc is about 0.1Ω-mm. The gate recess was formed using citric-acid-based enchants to selectively etch the highly-doped

InGaAs cap layer. After the D-mode gate recess etching, the gate recess region was treated by CF_4 plasma in an RIE system where the gate electrode and the plasma treated gate recess region were self-aligned. Then, Ti/Pt/Au gate metal was evaporated by e-beam and lifted-off with acetone. Following the plasma treatment, the device threshold voltage (Vth) was shifted and even changed from depletion-mode to enhancement-mode, with optimized treatment conditions.

Results and Discussion

Typical DC I-V characteristics of both D-mode and E-mode InAlAs/InGaAs MHEMTs are shown in Fig.1. After the gate recess regions were treated by CF_4 plasma with different RF power and time, the threshold voltage (Vth) of devices shifted positively. The Vth shifted from -0.7V to -0.05V after the gate recess regions were treated by CF_4 plasma with an RF power of 150W for 150 seconds. The peak g_m was 315mS/mm for the D-mode HEMT and 305 mS/mm for the E-mode device, respectively. As shown in Fig.2, the maximum drain current (I_{max}) was 330mA/mm for the D-mode and 220mA/mm for the E-mode MHEMTs, respectively. According to atomic force microscope (AFM) measurements shown in Fig.3, the thickness of InAlAs barrier layer was reduced by 0.6nm after CF_4 plasma treatment. Therefore, it can be concluded that the shift of threshold (Vth) was not due to the change of barrier layer thickness.

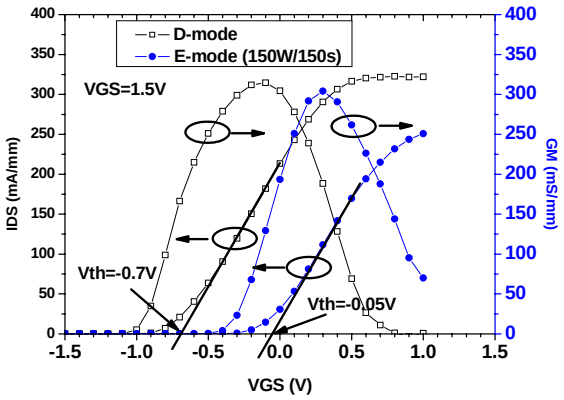

Fig.1 DC *I-V* transfer characteristics of D-mode and E-mode InAlAs/InGaAs MHEMTs with and without CF_4 treatment (RF power 150W for 150s to form E-mode).

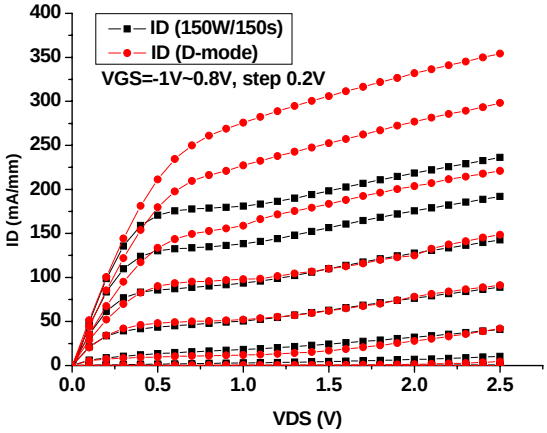

Fig.2. DC *I-V* output characteristics of E-mode InAlAs/InGaAs MHEMTs with and without CF_4 plasma treatment (RF power 150W and time 150s).

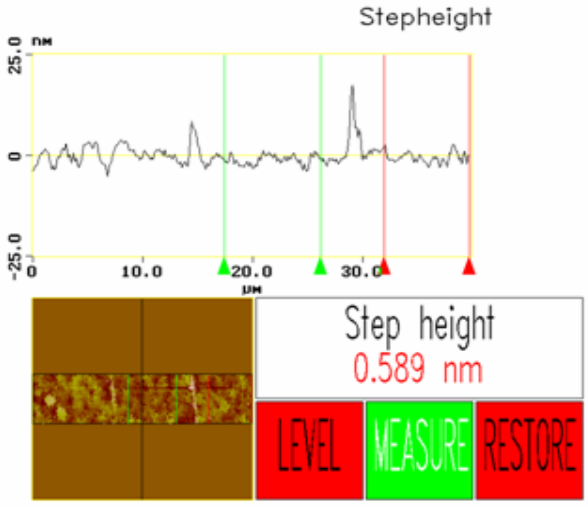

Fig.3 AFM image showing the insignificant etching effect of the CF_4 plasma treatment on the InAlAs layer.

Fig.4 shows gate currents of InAlAs/InGaAs MHEMTs after CF_4 treatments at different RF powers and times. The reverse-bias gate leakage currents were reduced after CF_4 plasma treatment compared to conventional MHEMTs without CF_4 plasma treatment. As the samples were treated by CF_4 plasma with 120W/120s, the gate leakage current decreased up to two orders of magnitudes at Vg=-3V. The current-gain cutoff frequency f_T and the maximum available gain f_{max} were calculated by extrapolating at -6dB/octave for the D-mode MHEMTs with a nominal gate length of 1.5μm. As shown in Fig.5, f_T was 17.9GHz and f_{max} was 80GHz.

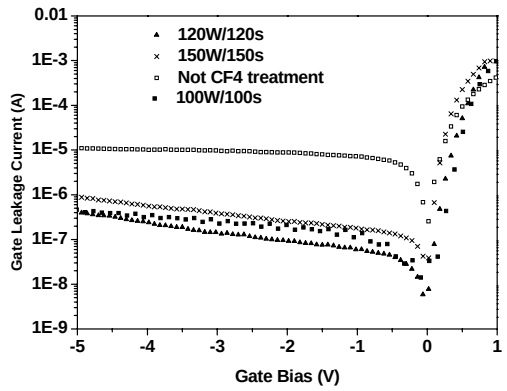

Fig.4 Gate currents of InAlAs/InGaAs MHEMTs with different plasma treatment conditions.

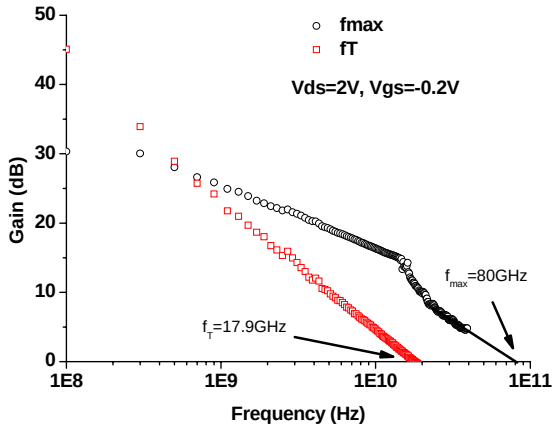

Fig.5 Current gain and maximum available gain for 1.5μm-gate D-mode MHEMTs with a gate width of 100μm.

CONCLUSIONS

In conclusion, we demonstrated a self-aligned CF_4 plasma treatment technique to fabricate E-mode InAlAs/InGaAs MHEMTs with reduced leakage current.

ACKNOWLEDGEMENTS

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ACRONYMS

MOCVD: Metalorganic Chemical Vapor Deposition
MHEMTs: Metamorphic High Electron Mobility Transistor
E/D-mode: Enhancement/Depletion-mode