# CMOS-on-Sapphire RF Switches for Cellular Handset Applications

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**Abstract**

**The need for integration of GSM, EDGE, and WCDMA in so-called WEDGE cellular handsets has disrupted the PIN diode and GaAs switch markets due to the performance, size, and cost requirements. This paper examines how UltraCMOS™ CMOS-on-Sapphire technology is monolithically solving the difficult performance challenges posed by this integration requirement, baselines it against competing GaAs solutions, and highlights the commercial success of the Technology. Last, this paper outlines the roadmap of continued scaling in device geometry, performance, and size.**

## INTRODUCTION

With nearly three billion subscribers world-wide and over 80% coverage of the world's population, cellular telephone coverage has been enabled through the creation of multiple frequency bands. Due to the stringent performance requirements dictated by the range needed for effective network operation, high selectivity filters are used liberally in handset front-ends. As the frequency band count continues to increase, handset designers incorporate switching elements to optimize the link budget. In this market, the highest volume consumer electronics market in the world, cost, performance, form-factor, and a long-term improvement roadmap become critical factors in a technology's success.

In the early days of GSM-only handsets, the industry was well served with PIN diodes due to their high performance and low cost. When the industry trajectory moved to convergence of GSM/EDGE and WCDMA, PIN diodes clearly did not meet the size and performance requirements of the next generation of handsets. Requiring long quarter-wave transmission lines and large forward bias currents to operate, PINs began to see their demise with the introduction of quad-band GSM.

To fill the technology gap created by the four-band requirement, in stepped IC-based solutions from UltraCMOS™ and GaAs. These technologies readily solved the multiple implementation problems with PIN diodes for multi-band operation and have essentially displaced PINs.

The addition of WCDMA to GSM/EDGE handsets has been heralded as the start of the 3G era, but introduced a new Technology gap with an onerous IP3 requirement of +68 dBm on the front-end switch for network robustness. This requires that the switch not generate a distortion signal larger than three trillionths of the WCDMA TX signal, the equivalent of one silicon atom in half-mile string of atoms. Meeting this difficult linearity requirement, UltraCMOS™ has emerged as the leading solution for RF front-end switching applications due to the benefits of a low-loss, low-capacitance Sapphire substrate combined with the fundamentally exceptional linearity of an intrinsic MOS device

## SUSTAINABLE COMPETITIVE ADVANTAGES

Converged 3G handset shipments supporting WEDGE exceeded 150M units in 2007, with projected volume shown in figure 1 exploding at a 50% CAGR in 2008 to beyond 500M units in 2011.

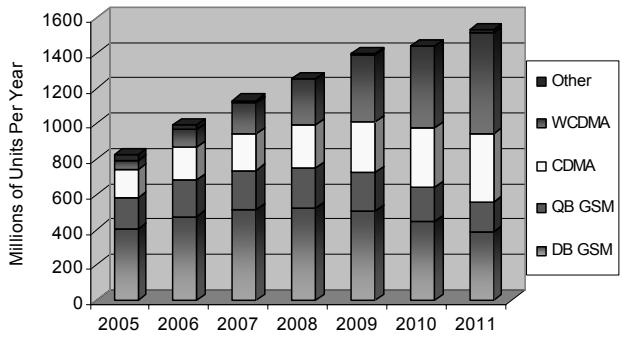


**Figure 1** – Global handset shipments by air interface

In 2007, the majority of 3G handsets shipped with quad-band GSM/EDGE and single-band WCDMA, requiring an SP7T switch. Due to 3G demand, the integration of three WCDMA bands is now required, increasing the switch complexity to an SP9T. This trend of increasing switch

complexity is expected to continue as there are now nine WCDMA bands defined with the number ever increasing.

To support WCDMA and GSM/EDGE simultaneously, the RF front-end switch is required to be the most linear element in the handset, and the most linear solid-state element of any high volume application in the world. Due to the insulating gate of a CMOS technology and the ability to natively incorporate mixed-signal design techniques, UltraCMOS™ devices are the only solid-state technology which can meet all performance requirements in a monolithic solution.

As the transistors on sapphire are dielectrically isolated from one another, they can be placed in series, or stacked, to tolerate the very high voltages levels present in an antenna switch. Although CMOS is low-voltage technology, peak-to-peak voltage handling of 50 V is readily tolerated. Additionally, on-chip bias generation provides for optimized performance and eliminates the need for external DC blocking capacitors.

A WEDGE SP9T implementation comparison between an UltraCMOS™ and GaAs is shown in Figure 2. Striking is the large difference in die sizes with the UltraCMOS™ die being 1.43 $mm^2$, approximately half the die size of the GaAs SP9T at 2.85 $mm^2$. With the fine design rules of aluminum metallization and the flexibility to place FETs in any orientation, the RF switches can be implemented more compactly that in GaAs. The complementary devices, analog control capability, and MOS capacitors allow for control of both series and shunt RF FETs with a simple four-wire interface and low current drain. Annotated in Figure 2 are the implementation areas of the 4:16 decoder of the two designs. The triple-metal process provides for placing flip-chip solder balls directly above circuitry, conserving die area.

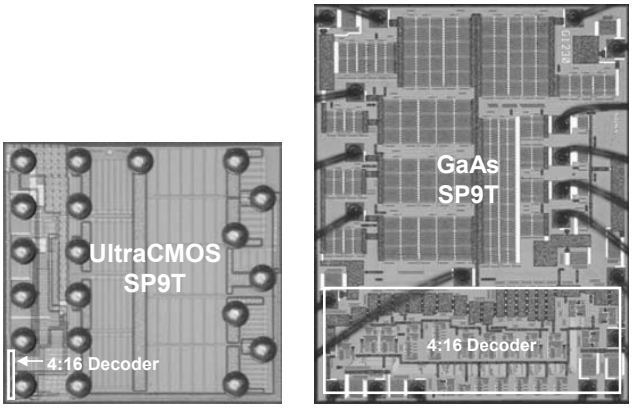


**Figure 2** – WEDGE SP9T switches in UltraCMOS™ and GaAs

The inclusion of shunting FETs on all ports thanks to complementary logic has tremendous impacts on ease of module design and performance. By controlling the impedances of the isolated ports at the plane of the switch ports, the module designer does not have to optimize all paths simultaneously, and intractable multi-variable problem, but can instead focus only on the active path. The shunt FETs also provide for very high isolation performance, relaxing the spurious requirements on transceivers. They also ensure protection of RX SAW filters from high RF power and ESD events.

ESD tolerance of UltraCMOS™ switches is exceptional due to the integration of ESD protection devices. With Class 2 (2000 V) HBM tolerance on control pins and 1500 V HBM tolerance on RF pins, UltraCMOS™ switches are highly robust against ESD damage. This reduces module fallout during manufacturing, and also dramatically reduces the required ESD circuitry at the antenna to meet the stringent IEC61000-4-2 requirement, recovering LTCC area and insertion loss.

Table 1 summarizes the SP9T performance of the two technologies. Insertion loss performance is approximately equal, while linearity performance of UltraCMOS™ far exceeds that of GaAs. The wide VDD range of UltraCMOS™ aligns with existing handset supply voltages, and bias generators are in development for direct operation from battery voltage or 1.8 V supplies.

TABLE I
Performance Comparison Between UltraCMOS™ and GaAs SP9Ts

| | **UltraCMOS™ SP9T** | **GaAs SP9T** |
|---|---|---|
| **Architecture** | True SP9T | SP5T+RX SP4T |
| **Insertion Loss** | **Nominal (dB)** | **Nominal (dB)** |
| TRX 865/1980 | 0.60 / 0.80 | 0.55 / 0.85 |
| TRX 960/2170 | 0.60 / 0.80 | 0.55 / 1.05 |
| TX 915/1910 | 0.60 / 0.75 | 0.50 / 0.75 |
| RX 960/1990 | 0.8 / 1.0 | 0.9 / 1.35 |
| **Harmonics** | **Nominal (dBm)** | **Nominal (dBm)** |
| TX 915 2fo/3fo @ +35 dBm | -50 / -50 | -36/-36 |
| TX 1910 2fo/3fo @ +33 dBm | -50 / -50 | -36/-36 |
| **Intermodulation Distortion** | **Nominal (dBm)** | **Nominal (dBm)** |
| TRX 849 IMD3 | -118 | -103 |
| TRX 2140 IMD3 | -112 | -88 |
| **DC Interface** | **Nominal** | **Nominal** |
| VDD Range | 2.4 - 3.2 V | 2.6 - 3.0 V |
| Current Drain | 100 uA | 360 uA |
| VIL | 0.4 V | 0.5 V |
| VIH | 1.4 V | 2.0 V |
| Decoder | Integrated 4:16 | Integrated 4:16 |

Although nominal VDD is specified for 2.75 V, integrated level shifting allows for 1.8 V and lower control logic to interface with scaled CMOS transceivers on the market, such as TI's LoCosto platform. This example shows a simple 4:16 decoder, but SPI-based serial programming is also available.

By using standard flip-chip CSP technology, UltraCMOS™ products significantly reduce the footprint of handset front-end modules (FEMs). Usually fabricated in costly LTCC, reductions in module area directly impact the total solution cost. In figure 3, migration from wirebonding to flip-chip reduced the LTCC substrate area consumed by 43% while simultaneously increasing the supported frequency band count from five to seven.

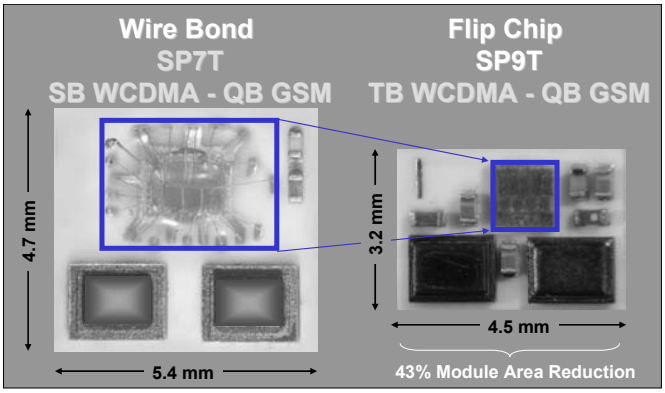


**Figure 3** – Size comparison between a wirebond SP7T-based pentaband module and flip-chip SP9T-based heptaband module

Employing flip-chip has an added benefit in that the switch can now be directly placed as an SMD component. As all other components in the FEM are SMDs, the need for any wirebonding equipment is eliminated. Shipped in tape-and-reel form, these flip-chip switches are placed on the module with standard placement machines, resulting in the lowest manufacturing cost. Additionally, at less than 250 µm mounted height, flip-chips reduce the overall module thickness, critical to meeting the demands for handset slimming.

The use of CMOS also readily allows for the use of mature advanced design tools for accurately predicting performance. Before first silicon arrives, multi-port S-parameter files can be generated from simulation for module design, reducing the number of module design spins required and accelerating market entry.

As a nearly lossless electrical insulator, Sapphire is ideally suited for passive integration. By depositing thick-film Cu as part of the flip-chip processing, very high-Q inductors can be created. On-chip MIM capacitors with Qs greater than 200 are including in the IC process. Figure 4 shows an example of passive integration with a switch. This SP6T integrated with dual TX LPFs monolithically integrates the functionality of a traditional LTCC-based quad-band GSM antenna switch module (ASM) in a 2.3 $mm^2$ area.

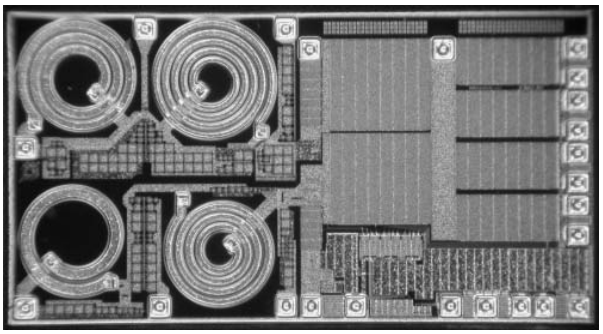

**Figure 4** – UltraCMOS™ SP6T with integrated TX PA harmonic LPFs

These advantages have culminated in rapid growth of UltraCMOS™ for RF switch applications in handsets. Figure 5 shows the exponential growth of UltraCMOS™ switch shipments into the handset market.

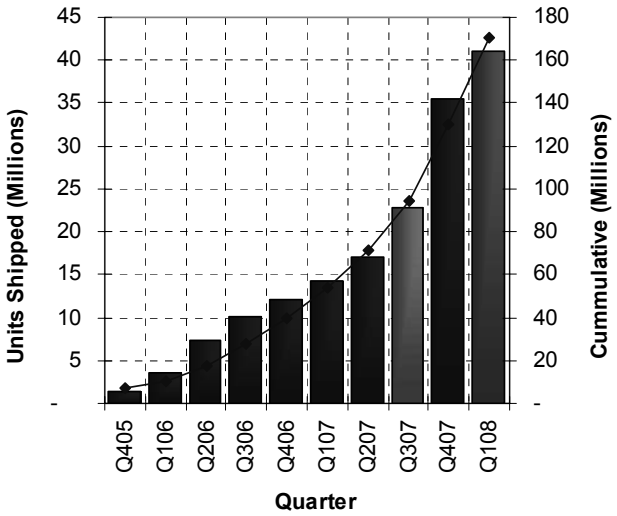


**Figure 5** – UltraCMOS™ handset switch shipments per quarter (bars) and cumulative (line)

With over 160M units shipped to date and a first quarter '08 run rate of nearly 500K units per day, UltraCMOS™ is making significant inroads into the growing 3G segment of the handset switch market.

## ULTRACMOS™ ROADMAP

UltraCMOS™ technology is today enabling the growth of 3G applications via legacy 0.5 um technology – ten times larger than State-of-the-Art production digital CMOS geometries. Switch products at the 0.35 um technology node are now ramping to production with improved performance and reduced die size. By following the ITRS scaling roadmap indicated in Figure 6, UltraCMOS™ is applying Moore's Law to the RF front-end, reducing area required per function and enabling further integration.

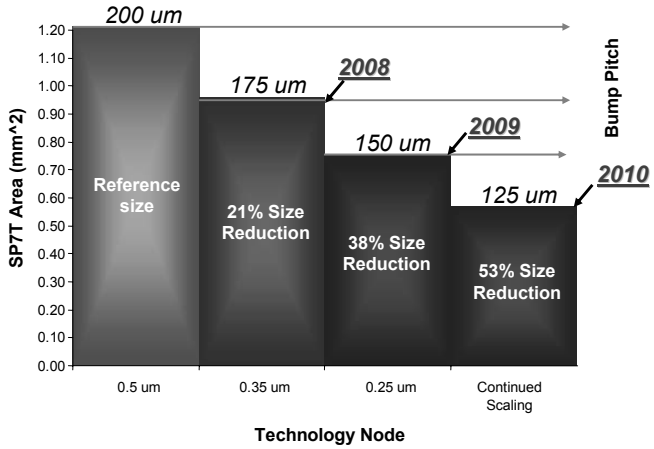


**Figure 6** – SP7T switch scaling vs. UltraCMOS™ Technology node

CMOS fabrication facilities are widely available at the legacy technology nodes shown in Figure 6, and CMOS-on-Sapphire is processed on the same equipment without modification. UltraCMOS™ has demonstrated its portability by being in mass production today in two fabrication facilities. The trajectory is towards the fabless relationship model which the silicon industry has embraced, and UltraCMOS™ will be in production in two additional Asian foundries by the end of 2008, bringing the total number of UltraCMOS™ production facilities to four.

## CONCLUSION

UltraCMOS™ RF switches provide tremendous value to handset front-ends, particularly in WEDGE applications functions where very high IP3 is required. These 3G handsets will continue to increase in complexity, requiring scaling to higher throw counts and even the integration of multiple switches on one die. These developments fully exploit the advantages of UltraCMOS™ and are increasingly difficult for GaAs. In conjunction with sapphire-based solid-state lighting, UltraCMOS™ consumption of sapphire is exploding and the supply chain is tracing the development and scaling of the silicon-substrate industry.