

# III-V on Silicon for Future High Speed and Ultra-Low Power Digital Applications: Challenges and Opportunities

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**Keywords:** III-V on silicon, quantum-well transistors, high speed, ultra-low power, digital logic

## Abstract

This presentation highlights the challenges and opportunities of III-V on silicon for future high speed, ultra-low power digital logic applications. It describes the heterogeneous integration of III-V transistors, such as enhancement-mode InGaAs quantum-well transistors on silicon substrates using thin composite buffer architecture, and their comparison to state-of-the-art silicon MOSFETs in device performance at very low supply voltage (e.g. 0.5V). The status of recent progress towards overcoming the *five grand challenges* in making III-V applicable for future logic applications is also discussed.

## INTRODUCTION

Recently there has been much interest generated in the research of non-silicon electronic materials and novel devices for future high-speed and ultra-low power logic applications [1-2]. Among the studied materials are carbon nanotubes [3], silicon nanowires [4], graphene [5], Ge [6] and III-V compound semiconductors such as InSb [7-8] and InGaAs [9-10]. These materials, in general, have significantly higher intrinsic (p or n) mobility than silicon, and they have the potential for enabling future high speed digital applications at very low supply voltages. Of all these non-Si materials, III-V and Ge are the most mature and practical, with the former having been used in commercial communication and optoelectronic products for a long time. Among the III-V systems of interest, InSb has the highest electron mobility of 20,000-30,000  $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$  at sheet carrier density of  $1.3 \times 10^{12} \text{ cm}^{-2}$  [7-8], while InGaAs has electron mobility of 10,000  $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$  at sheet carrier density of  $3.5 \times 10^{12} \text{ cm}^{-2}$  [9-10]. Both these systems show improved energy-delay product, which represents the energy efficiency of the device, over silicon as shown in Fig. 1 [1, 11]. Recently very high-speed InSb and InGaAs quantum-well (QW) transistors with 80nm physical gate length have been demonstrated at a low supply voltage of only 0.5V [7, 9]. Compared with state-of-the-art silicon MOSFETs, these III-V QW transistors show either a 1.5-fold improvement in intrinsic speed performance at the same power, or 10-fold reduction in power for the same speed performance. As these channel

materials have a low bandgap, quantum-well device structures, in which carriers are confined in a low band-gap material by adjacent barrier layers with a larger bandgap, are required to control the transistor parasitic junction leakage and off-state leakage. Although these III-V devices show very attractive and tangible merits, many technical challenges need to be overcome before they will become applicable for future high speed and low power digital applications. Specifically there are 5 major technical challenges, *the five grand challenges*, which need to be overcome before III-V will play a major role along with Si for future digital logic applications [11].

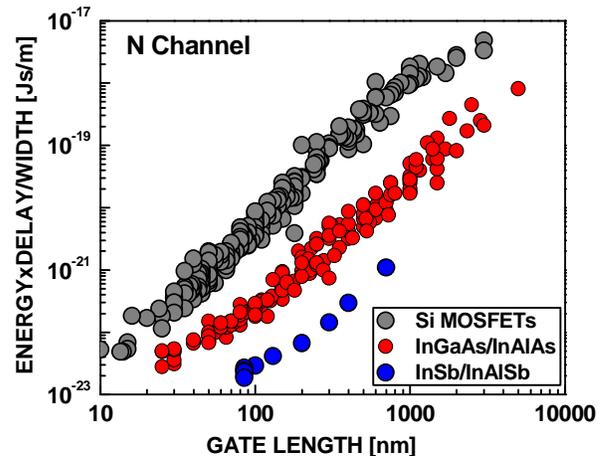


Figure 1: Normalized energy-delay product of n-channel InSb and InGaAs quantum-well transistors compared with that of standard silicon MOSFETs [refs.1, 11].

## THE FIVE GRAND CHALLENGES

The 5 major technical challenges that need to be overcome include:

- 1) Heterogeneous integration of III-V device layers on silicon substrate: III-V materials will need to be integrated onto Si as the high-mobility channel materials for future high speed and low power logic transistors. The composite buffer layer between the III-V transistor and silicon substrate needs to act as an effective filter for defects, and it also needs to be

sufficiently thin without degrading mobility for cost reduction and ease of integration with Si CMOS devices on the same wafer.

- 2) Enhancement-mode III-V transistors: Enhancement-mode III-V devices with the right threshold voltages are required for acceptably-low off-state transistor leakage ( $I_{OFF}$ ) when the gate voltage is off. This is important for low power digital logic application which requires low  $I_{OFF}$  and high  $I_{ON}/I_{OFF}$  ratio.
- 3) A gate dielectric stack compatible with III-V: Due to the lack of a stable gate dielectric stack, currently all III-V QW devices use a direct Schottky metal gate, which results in a large parasitic gate leakage. A gate dielectric stack which is compatible with III-V materials will be needed to solve this problem. Formation of an unpinned dielectric/semiconductor interface has been particularly challenging for III-V and it is critical towards achieving a stable gate dielectric stack on these materials.
- 4) A viable p-channel transistor for CMOS configuration: Currently the hole mobility in III-V materials is not high enough for III-V CMOS application. One solution involves improving hole mobility in III-V by incorporating bi-axial strain and/or uni-axial strain in the device channel. Another alternative is exploring the use of other high-mobility materials, such as Ge quantum-well systems, for the p-channel transistor. The right material should exhibit hole mobility of  $>3000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  at sheet carrier density  $>3 \times 10^{12} \text{ cm}^{-2}$ .
- 5) Transistor scalability: For III-V devices to be competitive versus scaled Si MOSFETs, their physical gate lengths need to be scaled to 35nm and below with acceptably-low  $I_{OFF}$  ( $<100\text{nA}/\mu\text{m}$ ) and high  $I_{ON}/I_{OFF}$  ratio ( $>1000$ ) at supply voltage of 0.5V. This will require i) enhancement-mode operation, ii) high-K gate dielectrics with sufficiently thin equivalent oxide thickness for improving short-channel performance, and perhaps iii) a non-planar, multi-gate transistor structure [1] to improve device electrostatics with scaling.

## RECENT PROGRESS

Recently good progress has been made by both industry and academic research groups towards solving the technical problems and overcoming the challenges. For instance, high-performance depletion-mode InSb and InGaAs QW transistors have been fabricated on silicon substrates [8-9]. Heterogeneous integration of enhancement-mode InGaAs QW transistor on silicon substrate using thin ( $1.3\mu\text{m}$ ) composite buffer architecture has been demonstrated for high-speed and low-power logic applications at supply voltage of only 0.5V [10]. ALD high-K gate dielectrics have been deposited on InGaAs substrate with encouraging results

[12]. Hole mobility has been improved in III-V material systems using bi-axial strain, with hole mobility of  $>1000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  at sheet carrier density of  $\sim 1.6 \times 10^{12} \text{ cm}^{-2}$  demonstrated [13]. The scaling behavior of InGaAs HEMT has been studied for logic applications with positive outlook [14]. 40nm InAs HEMTs have been fabricated for logic applications with  $I_{ON}/I_{OFF} > 10,000$  demonstrated with a 0.5V gate voltage ( $V_G$ ) swing [15]. Although we are still far away from solving all the technical issues, all these research results are important milestones which help drive towards the goal of making III-V on silicon practical for future high speed and ultra-low power digital applications.

## ENHANCEMENT-MODE III-V DEVICE ON SILICON

Of the 5 grand challenges, 1) and 2) have made the most progress so far. Recently InGaAs QW structure has been successfully integrated onto Si substrate using a novel, thin composite metamorphic buffer architecture with total buffer thickness scaled down to  $1.3\mu\text{m}$ , resulting in high-performance 80nm enhancement-mode InGaAs QW transistor on silicon, as shown in Figure 2 [10]. Comparing to the Si n-MOSFET, the enhancement-mode III-V device on Si exhibits  $>10\text{X}$  reduction in DC power dissipation for the same speed performance or  $>2\text{X}$  gain in speed performance for the same power as shown in Figure 3. The key points of this III-V on Si demonstration are i) the composite buffer layer thickness can be scaled from  $>3.0\mu\text{m}$  to  $1.3\mu\text{m}$  without degrading channel mobility as shown in Fig. 4, ii) parasitic, parallel conduction in heterogeneous integrated systems can be eliminated as shown in Fig. 5, and iii) the III-V quantum-well layer in the system can be made virtually defect-free [10]. In addition to enabling future high-speed and ultra-low power logic applications, successful integration of III-V on silicon can open up opportunities for new functionalities such as integrating logic, optoelectronic and communication platforms on the same silicon wafer.

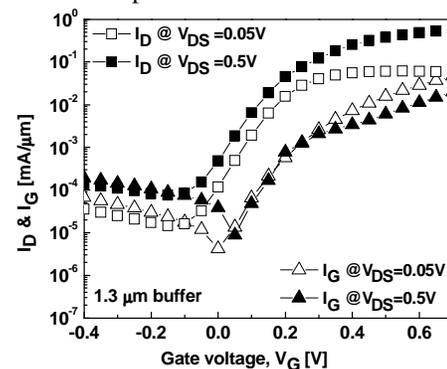


Figure 2: Drain current ( $I_D$ ) and gate leakage ( $I_G$ ) versus gate voltage ( $V_G$ ) of enhancement-mode  $L_G=80\text{nm}$   $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  QWFET on Si with  $1.3\mu\text{m}$  composite buffer at room temperature.  $V_T = +0.11\text{V}$ ,  $I_{Dsat} = 0.32\text{mA}/\mu\text{m}$ ,  $I_{ON}/I_{OFF} = 2150$  at  $V_{DS}=0.5\text{V}$  with  $0.5\text{V}$   $V_G$  swing [ref. 10].

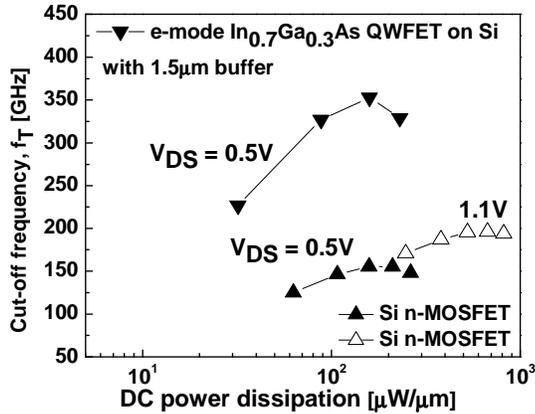


Figure 3: Cut-off frequency as a function of DC power dissipation for the enhancement-mode  $L_G=80\text{nm}$   $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  QWFET on Si with  $1.5\mu\text{m}$  composite buffer at  $V_{DS}=0.5\text{V}$ , versus standard Si n-MOSFET transistor with  $L_G = 60\text{nm}$  at  $V_{DS}=0.5\text{V}$  and  $1.1\text{V}$  [ref. 10].

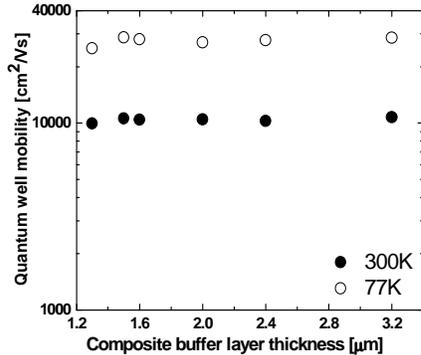


Figure 4:  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  QW electron mobility versus composite buffer layer thickness on Si at 300K and 77K. No mobility degradation is observed, indicating that the metamorphic buffer architecture is effective in filtering dislocations [ref. 10].

## CONCLUSION

III-V devices have shown some very attractive and tangible merits, but there exist many difficult challenges to overcome before they will become applicable for future high speed, ultra-low power logic applications. Although we are far away from solving all the issues, good progress has been made so far by various research groups in industry and academia. The recent demonstration of high performance and low power enhancement-mode III-V transistors on silicon via a thin composite metamorphic buffer layer has generated much excitement. Furthermore, III-V on Si can open up new opportunities of integrating new features and functionalities on silicon. Going forward, research of III-V on silicon will be more exciting and rewarding than ever.

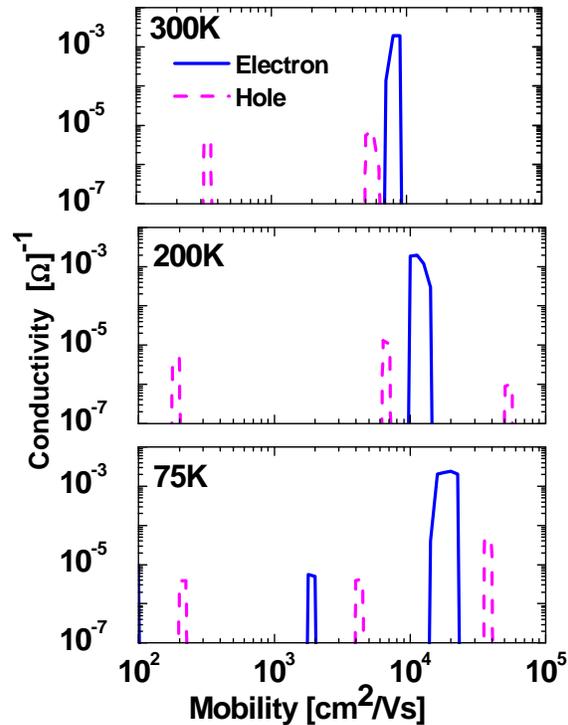


Figure 5: Quantitative mobility spectrum analysis (QMSA) for  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  QW on Si at different temperature indicating no parallel, parasitic conduction to the active  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  channel [ref. 10].

## REFERENCES

- [1] R. Chau, B. Doyle, S. Datta, J. Kavalieros and K. Zhang, "Integrated nanoelectronics for the future," *Nature Materials*, Vol. 6, Nov 2007, pp. 810-812.
- [2] R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz and M. Radosavljevic, "Benchmarking Nanotechnology for High-Performance and Low-Power Logic Transistor Applications," *IEEE Transactions on Nanotechnology*, Vol. 4, No. 2, March 2005, pp.153-158.
- [3] S.J. Wind, J. Appenzeller, R. Martel, V. Derycke and P. Avouris, "Vertical Scaling of Carbon Nanotube Field-Effect Transistors Using Top Gate Electrodes," *Appl. Phys. Lett.*, vol. 80, 2002, pp.3817-3819.
- [4] M. Lieber, "Nanowires as Building Blocks for Nanoelectronics and Nanophotonics," *International Electron Devices Meeting (IEDM) Technical Digest*, 2003, pp. 300-302.
- [5] W. A. de Heer, C. Berger, E. Conrad, P. First, R. Murali and J. Meindl, "Pionics: the Emerging Science and Technology of Graphene-based Nanoelectronics," *IEDM Technical Digest*, 2007, pp. 199-202.
- [6] Y. Kamata, "High-k/Ge MOSFETs for future nanoelectronics," *Materials Today*, Vol. 11, No. 1-2, Jan-Feb 2008, pp. 30-38.

[7] S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T.J. Phillips, D. Wallis, P. Wilding and R. Chau, "85nm Gate Length Enhancement and Depletion mode InSb Quantum Well Transistors for Ultra High Speed and very Low Power Digital Logic Applications," IEDM Technical Digest, 2005, pp. 783-786.

[8] T. Ashley, L. Buckle, S. Datta, M.T. Emeny, D.G Hayes, K.P. Hilton, R. Jefferies, T. Martin, T.J. Philips, D.J. Wallis, P.J. Wilding and R. Chau, "Heterogeneous InSb quantum well transistors on silicon for ultra-high speed, low power logic applications," Electronics Letters, Vol. 43, No. 14, July 2007.

[9] S. Datta, G. Dewey, J. M. Fastenau, M. K. Hudait, D. Loubychev, W. K. Liu, M. Radosavljevic, W. Rachmady and R. Chau, "Ultrahigh-Speed 0.5 V Supply Voltage In<sub>0.7</sub>Ga<sub>0.3</sub>As Quantum-Well Transistors on Silicon Substrate," IEEE Electron Device Letters, Vol. 28, No.8, 2007, pp. 685-687.

[10] M.K. Hudait, G. Dewey, S. Datta, J.M. Fastenau, J. Kavalieros, W.K. Liu, D. Lubyshev, R. Pillarisetty, W. Rachmady, M. Radosavljevic, T. Rakshit and Robert Chau, "Heterogeneous Integration of Enhancement Mode In<sub>0.7</sub>Ga<sub>0.3</sub>As Quantum Well Transistor on Silicon Substrate using Thin ( $\leq 2\mu\text{m}$ ) Composite Buffer Architecture for High-Speed and Low-Voltage (0.5V) Logic Applications," International Electron Devices Meeting (IEDM) Technical Digest, 2007, pp. 625-628.

[11] R. Chau, S. Datta, A. Majumdar, "Opportunities and Challenges of III-V Nanoelectronics for Future High-speed, Low-power Logic Applications," Technical Digest, IEEE Compound Semiconductor Integrated Circuit Symposium, Palm Springs, CA., Nov. 2005, pp. 17-20.

[12] Y. Xuan, Y.Q. Wu, T. Shen, T. Yang and P.D. Ye, "High performance submicron inversion-type enhancement-mode InGaAs MOSFETs with ALD Al<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub> and HfAlO as gate dielectrics," IEDM Technical Digest, 2007, pp. 637-640.

[13] J.B. Boos, B.R. Bennett, N.A. Papanicolaou, M.G. Ancona, J.G. Champlain, R. Bass and B.V. Shanabrook, "High mobility p-channel HFETs using strained Sb-based materials," Electronics Letters, Vol. 43 No. 15, July 2007.

[14] D-H. Kim and J. del Alamo, "Scaling Behavior of In<sub>0.7</sub>Ga<sub>0.3</sub>As HEMTs for Logic," International Electron Devices Meeting (IEDM) Technical Digest, 2006, pp. 837-840.

[15] D-H. Kim and J. del Alamo, "Logic Performance of 40nm InAs HEMTs," IEDM Technical Digest, 2007, pp. 629-632.