The DARPA COmpound Semiconductors on Silicon (COSMOS) Program

Dr. Mark J. Rosker

Defense Advanced Research Projects Agency, 3701 North Fairfax Drive, Arlington, VA 22203-1714
mark.rosker@darpa.mil, 571-218-4507

***Abstract* — The COmpound Semiconductors on Silicon (COSMOS) program sponsored by the Defense Advanced Research Projects Agency (DARPA) is developing heterogeneous integration processes to enable the "transistor-scale" integration of compound semiconductors with silicon. This talk will review the program goals, discuss its implications, and present early results.**

***Key Words* — Si CMOS, heterogeneous integration, compound semiconductors.**

I. Introduction

The development of compound semiconductor electronics has been motivated by their unique materials properties relative to silicon. If both narrow bandgap (e.g., InP, ABCS) and wide bandgap (e.g., GaN, SiC, GaP) materials are considered, these properties include lower operating voltages, higher breakdown voltages, superior thermal conductivity, direct bandgap optical transitions, etc. Nonetheless, III-V's have failed to displace Si in all but the most specialized of electronic applications. This fact is attributable to the aggressive device scaling and the extremely high-scale integration that has characterized Si electronics development. Even for RF applications, where compound semiconductors have most commonly found application, the advantages of compound semiconductors have been eroded by advances in silicon and SiGe devices. Recent research, including that supported by the Defense Advanced Research Projects Agency (DARPA) in its Technology for Efficient, Agile Mixed-Signal Microsystems (TEAM) program, have driven the RF performance of silicon-based electronics well beyond what was previously thought realizable. Given these trends, it has been increasingly clear that the future of III-V electronics depends not on displacing Si, but rather on heterogeneous integration of compound semiconductors with silicon.

Currently, heterogeneous integration of compound semiconductors with silicon is typically achieved through the use of multi-chip modules and similar assemblies. While adequate for relatively low performance applications (e.g., power amplifiers for cellular telephone handsets), the integration complexity that can be achieved in this manner is extremely limited.

The DARPA COmpound Semiconductors on Silicon (COSMOS) program is developing a heterogeneous integration technology which will overcome these limitations, enabling heterogeneous integration at micron distance scales. If this vision can be achieved routinely and at low cost, it will allow circuits in which every device is optimized for its specific function. This capability would have a revolutionary impact on the performance of both military and commercial circuits and would dramatically impact the compound semiconductor community.

II. COSMOS Program Objectives

The objective of the COSMOS program is to develop a viable process for the "transistor-scale" heterogeneous integration of compound semiconductor (CS) with standard Si CMOS and to establish that this integration enables superior performance in specific mixed-signal circuit demonstrators. The COSMOS program is developing methods to integrate transistors from at least one CS semiconductor technology together with transistors on a wafer fabricated using a standard Si CMOS foundry process. This must be achieved without any extraordinary modifications (i.e., one that would not be transparent to a Si foundry) of the Si CMOS process.

Specific end-of-program goals include heterogeneously integrated circuits with the following characteristics:

- CS and Si-based transistors placed in very close proximity (≤ 5μm minimum interconnect length)
- Tight pitch (≤ 5μm minimum separation) of the heterogeneous interconnect vias (i.e., those connecting CS and Si-based transistors)
- High yield of the heterogeneous interconnects (≥ 99.99%)
- Circuit robustness

- Minimal performance degradation of the CS and Si-based devices as a result of the integration process (< 10% reduction in transconductance)

III. Approach And Technical Challenges

The COSMOS program is exploring several integration strategies to ascertain which is the most successful in terms of performance, size and cost. One approach, pursued by a team led by Northrop-Grumman, involves sub-circuit integration in which III-V devices are placed onto a processed CMOS wafer. At the other end of the spectrum, epitaxial methods are being explored to grow III-Vs onto silicon substrates; this is the approach being developed by a Raytheon team. An intermediate approach is also being studied by a group led by HRL Laboratories.

Key technical challenges being addressed in the program include:

(1) *Placement of CS Devices*: A central problem is the capability to manufacture, position, register, and align "chiplets" (~several μm on a side) of CS on a Si substrate.

(2) *Heterogeneous Material Interfaces*: A successful COSMOS implementation must address the coefficient of thermal expansion (CTE) mismatch which can be expected to occur at this interface and potentially degrade device performance.

(3) *Dense Heterogeneous Interconnects:* To enable fine-scale integration, interconnects and vias must be placeable with very short (~several μm) pitch separations without excessive electrical losses and while maintaining high electrical isolation. .

(4) *Yield Enhancement:* A high yield COSMOS process will be critical to enable the routine fabrication of heterogeneous integrated circuits with high reliability and low cost. The ultimate yield goal of the COSMOS technology is to match that of the commercial Si technologies.

In the first Phase of this program the performers are focusing transistor-scale integration technology, to develop and demonstrate a viable process technology to integrate CS and Si CMOS transistors on a very short size-scale within a small circuit. The demonstration circuit will be a heterogeneously integrated differential amplifier will provide both approach proof of concept, and outstanding characteristics compared to today's state of the art.

Phase II focuses on yield enhancement and circuit integration. The objectives of this phase are to significantly improve both the yield and the density of the heterogeneous interconnect process, the latter achieved through a significant reduction in the pitch of the heterogeneous interconnects. The specific circuit demonstrator to validate performance will be a circuit related to the simple differential amplifier in Phase I but at a much higher level of circuit complexity: a heterogeneously-integrated 13-bit digital-to-analog converter (DAC).

Finally, in Phase III the performers will demonstrate advanced heterogeneous circuits. The objective of this phase is to scale the COSMOS process to a much larger circuit, conclusively demonstrating that fine-scale heterogeneous integration can be realized on a large scale. The specific circuit demonstrator to validate performance will be a heterogeneously-integrated 16-bit analog-to-digital converter (ADC).

Table 1 shows the minimal set of GNG metrics which must be achieved by the conclusion of each phase.

TABLE I

Heterogeneous Interconnect Length (1)	μm	≤ 5	≤ 5	≤ 5
Heterogeneous Interconnect Pitch (2)	μm	≤ 25	≤ 5	≤ 5
Heterogeneous Interconnect Yield (3)	%	≥ 99	≥ 99.9	≥ 99.99
Demonstration Circuit		**Differential Amplifier** • *Slew rate ≥ 10^4 V/μsec* • *Voltage swing ≥ 3V* • *DC gain * Unity-gain BW ≥ 10^4 V/V- GHz* • *Power ≤ 100mW*	**D/A Converter** • *Resolution ≥ 13 bits* • *SFDR ≥ 78 dBc (@ f_{output} = 1±0.25 GHz)* • *Power ≤ 2.5 W*	**A/D Converter** • *16 SNR bits* • *500MHz BW* • *SFDR ≥ 98 dBc* • *Power ≤ 4W*
Circuit Robustness (4)	%	≥ 50	≥ 95	≥ 95
Other Milestones				
CS Transistor Performance (5)	%	≥ 80	≥ 90	≥ 90
Si CMOS Transistor Performance (6)	%	≥ 80	≥ 90	≥ 90
Demo Circuit RF Yield (7)	%	≥ 25 (8)	≥ 50 (9)	≥ 50 (8)

1. Minimum interconnect length between CS and Si-based transistors

2. Minimum lateral distance between heterogeneous interconnect vias

3. Yield calculated for a single heterogeneous interconnect; must be validated by a proposed-defined test circuit containing a large number of daisy-chained heterogeneous interconnects

4. Fraction of yielded circuits which remain yielded after 100 temperature cycles over a baseplate temperature range from –55°C to 85°C with dwell-time at each temperature extreme of at least ten minutes

5. The ratio of the transconductance of CS transistors after the COSMOS integration process to that of the same type of CS transistors fabricated by the same process on a CS substrate

6. The ratio of the transconductance SI CMOS transistors after the COSMOS heterogeneous integration process to that of similar transistors without such integration

7. The fraction of functional circuits achieving all GNG requirements simultaneously

8. Circuits from a single wafer containing at least 20 demo circuits

9. Circuits from a lot of at least three wafers each containing at least 20 demo circuits

IV. Potential Impact

One critical example of COSMOS will be in the demonstration of mixed-signal circuits, such as analog-to-digital converters (ADCs), with outstanding circuit characteristics. Based on exploiting the unique properties of multiple but disparate semiconductor materials, the technologies developed under COSMOS will enable the design and manufacture of high performance, cost-effective, embeddable integrated components such as the analog-to-digital converters, with large dynamic ranges (16 bits), large signal bandwidths (500 MHz), and low in power dissipation (4 W). COSMOS technologies will enable systems that have greater range, larger bandwidths and better sensitivities, with lower false alarms and power dissipation.

Other applications of COSMOS may include high power amplifiers (e.g., GaN w/ CMOS) and integrated photonics (e.g., InP, ABCS, or GaP w/ CMOS).

V. Conclusion

The DARPA COSMOS program is developing a heterogeneous integration technology at micron distance scales. The three performers on this program are approaching these technical challenges monolithically, by assembly, and in between. The program focuses on three demonstration circuits, a differential amplifier, a DAC, and an ADC in the final Phase. If this vision can be achieved routinely and at low cost, it will allow circuits in which every device is optimized for its specific function. This capability would have a revolutionary impact on the performance of both military and commercial circuits and would dramatically impact the compound semiconductor community, enabling systems that have greater range, larger bandwidths and better sensitivities, with lower false alarms and power dissipation.

VI. Acknowledgements

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VII. Acronyms

COSMOS: COmpound Semiconductor Materials On Silicon
DARPA: Defense Advanced Research Projects Agency
CMOS: Complementary metal-oxide-semiconductor
RF: Radio Frequency
CS: Compound Semiconductor
TEAM: Technology for Efficient, Agile Mixed-Signal Microsystems
CTE: Coefficient of Thermal Expansion
DAC: Digital to Analog Converter
ADC: Analog to Digital Converter