

# Reliability and MMIC Technology Development and Production

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## Abstract

A key aspect of MMIC technology development and production is reliability. At Northrop Grumman Space Technology (NGST), reliability assessment and improvement are incorporated into the formative stages of technology development and continue through process qualification and manufacturing. Key components of this approach include: multi-temperature accelerated life testing; other accelerated life testing; determination of failure mechanisms using both device parametric changes and destructive physical analysis; investigation of anomalous behavior or unexpected failures; and the use of long-term, low-temperature testing. The importance of each of these components will be illustrated using the results from GaAs HEMT MMIC technology. Multi-temperature testing projects GaAs HEMT MMIC life times in excess of  $10^9$  hours at a junction temperature of  $125^\circ\text{C}$  or less. Investigation of the reliability test failures demonstrates the primary failure mechanism for thermally accelerated failures is gate-sinking. In addition, hot-carrier induced degradation can limit MMIC life times and must be tested for differently than thermally-accelerated mechanisms. Investigation of anomalous behavior led to the identification a previously unidentified failure mechanism related to movement/loss of the ohmic metal. Long-term, low-temperature testing displays excellent stability and provides confidence in the inherent reliability of technology.

## INTRODUCTION

A comprehensive approach to ensuring MMIC reliability, shown schematically in Figure 1, involves incorporating reliability assessment and improvement into the formative stages of technology development and continuing those activities throughout process qualification and manufacturing. Key components of this approach include: multi-temperature accelerated life testing; other accelerated life testing; determination of failure mechanism using both device parametric changes and destructive physical analysis; investigation of anomalous behavior or unexpected failures; and the use of long-term, low-temperature testing. The importance of each of these components will be illustrated using the results from GaAs HEMT MMIC technologies.

## MMIC Technology Quality & Reliability Approach

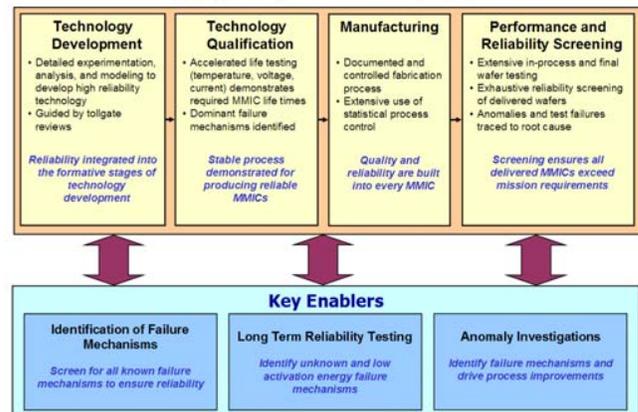


Figure 1. NGST's approach to MMIC reliability.

## GAAS HEMT TECHNOLOGY

The GaAs HEMT technology described in this paper uses a  $0.15 \mu\text{m}$  Ti/Pt/Au T-gate [1]. The epitaxial structure contains an  $\text{In}_{0.22}\text{Ga}_{0.78}\text{As}$  channel clad on both sides with  $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$  barriers as shown in Figure 2.

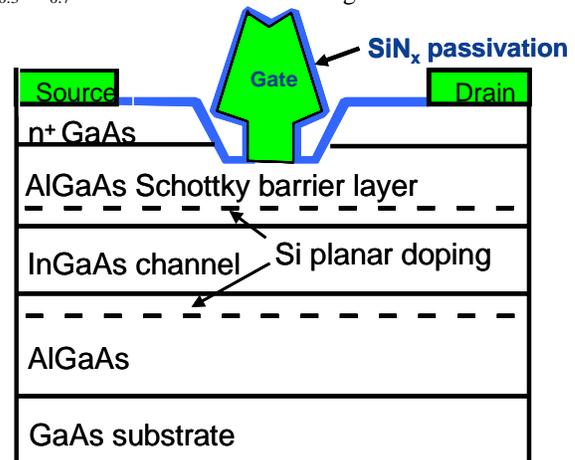


Figure 2.  $0.15 \mu\text{m}$  GaAs HEMT.

## MULTI-TEMPERATURE LIFE TEST

High-temperature life testing is the primary method for estimating MMIC life times at operating conditions. This is

typically a 3 temperature life test with ambient temperatures at 200°C and above. This method is described in various industry standards documents, including MIL-STD-883 and JEP118 (where a 4th temperature requirement is outlined). An excellent test vehicle for this testing is a 2-stage, 40 GHz GaAs HEMT amplifier MMIC. This MMIC provides both RF output characteristics and aggregate DC device parametric data (for example, Gm and Id versus Vg, as shown in Figure 3). During life test the parts are stressed while biased at maximum voltage and current allowed (5V and 250 mA/mm). Between stress intervals, the MMICs are characterized for both RF performance and aggregate DC device parameters.

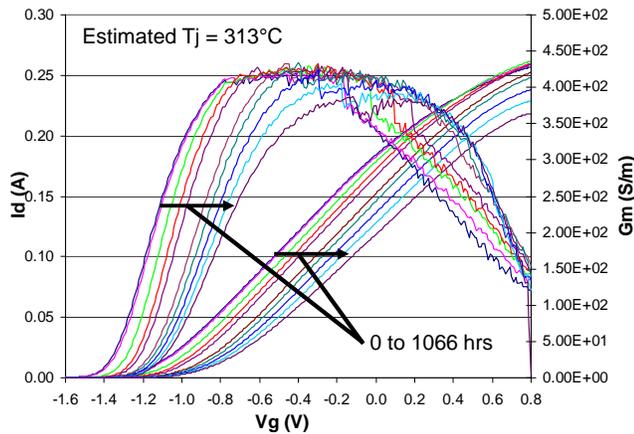


Figure 3. Aggregate device parametric data as amplifier is stressed from 0 to 1066 hours.

The multi-temperature life test data for GaAs HEMT is fit fairly well by a log-normal distribution and a single activation energy as shown in Figure 4. Wafer-to-wafer variation is the primary sources of non-ideal behavior. The life test results ( $\ln\text{-sigma} = 0.47$ ,  $E_a = 1.5 \pm 0.1$  eV,  $\text{MTF} = 1.3 \times 10^9$  hrs) shown in Figure 5 provide confidence in life time projections to operating conditions

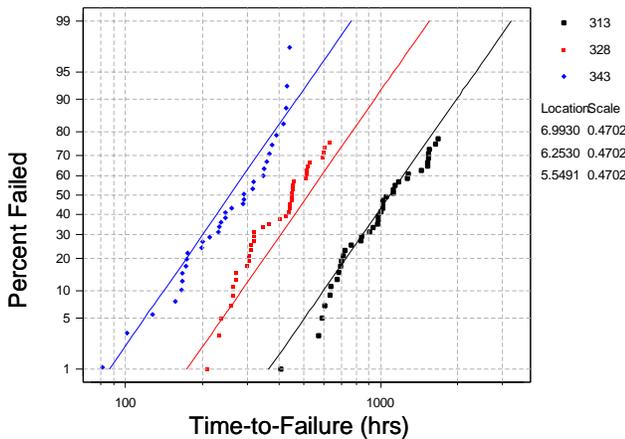


Figure 4. GaAs HEMT failure times fit with log-normal distribution.

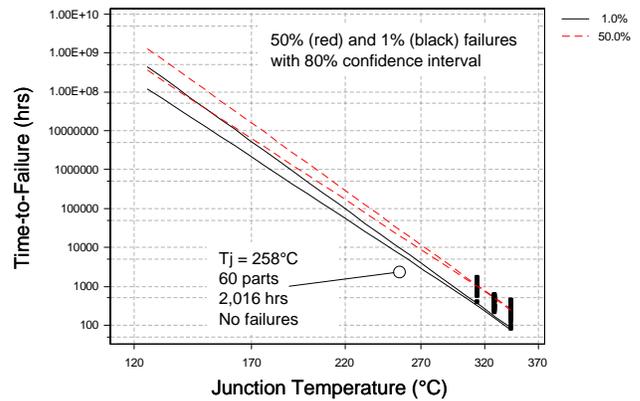


Figure 5. Arrhenius fit to life test data projecting MTF >  $10^9$  hours at  $T_j = 125^\circ\text{C}$ .

#### OTHER ACCELERATED LIFE TEST

Failure mechanisms have been identified in III-V compound devices that have weak to negative thermal acceleration. Special testing needs to be conducted to estimate the impact of such mechanisms, when present, on MMIC life times during operation. For GaAs HEMT devices, hot electron effects can lead to reduced power output over operating life. Extensive testing was conducted to create an empirical model for these effects [1]. Design rules and as-built product screens are used to ensure installed parts meet life time requirements.

#### FAILURE MECHANISMS

In analyzing failure data, it is important to establish that the same failure mechanism is causing the observed degradation. Determination of failure mechanism uses both device parametric changes measured during testing and destructive physical analysis conducted after testing is complete. Failure mechanisms are identified from internal research and review of industry published results. Extensive experimentation, analysis, and life testing are conducted to identify failure mechanisms. Identification begins in the technology development phase and continues throughout manufacturing.

For high-temperature GaAs HEMT testing, two failure signatures are observed. The first is a gradual decrease in  $\Delta S_{21}$  associated with Gm and Id shift toward positive Vg. The STEM cross-section for this signature shows the gate metal diffusion toward the channel (Figure 6) [2]. The second is a very rapid decrease in  $\Delta S_{21}$ , typically after a gradual decrease of 1 dB, resulting in channel shorting. The STEM cross-section shows gate metal diffusion into the channel region (Figure 7). Hot electron induced degradation is an equally important failure mechanism for devices operated under high RF drive [1].

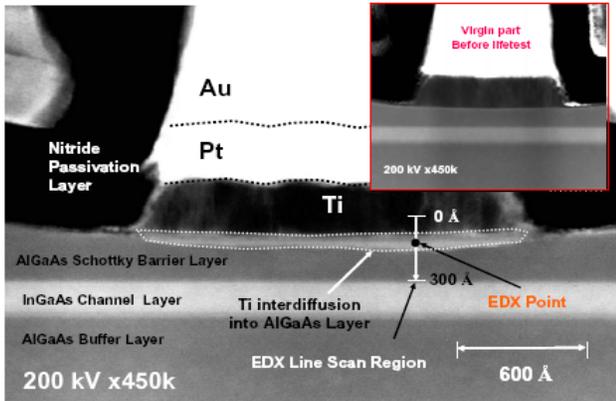


Figure 6. STEM cross-section of gate region shows gate sinking into barrier layer.

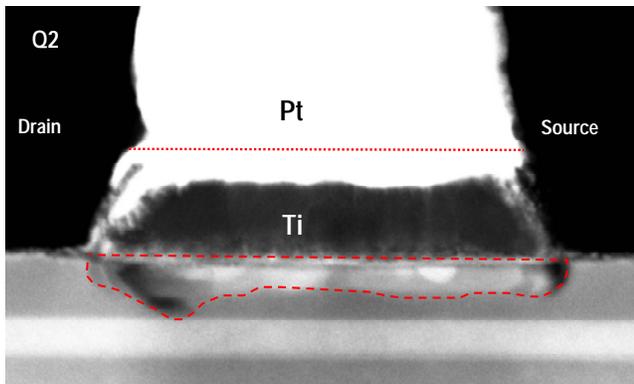


Figure 7. STEM cross-section of gate region shows gate sinking into channel layer.

#### ANOMALOUS BEHAVIOR OR UNEXPECTED FAILURES

Reliability testing invariably results in some unexpected failures or other anomalous behavior (field returns of MMICs are also an important record of anomalous behavior). When observed, it is important to investigate the source of the anomalous behavior. Common sources of anomalous behavior include equipment and test issues (such as transient overstresses); handling and assembly issues (such as ESD), and previously unidentified failure mechanisms. Obviously, failures that are determined to be due to something other than reliability degradation should be removed or censored in the data set.

Investigation of GaAs HEMT anomalous behavior led to the identification a previously unidentified failure mechanism. Initial qualification wafers displayed an unusual change in the device parametric data. The drain-source resistance increased significantly as opposed to expected  $G_m/I_d$  changes (due to gate sinking shown in Figure 3). Destructive physical analysis revealed extensive movement/loss of the ohmic metal as shown in Figure 8. Investigation identified stress in the metal stack (due to recent change in a layer thickness in the stack) as the likely source of this failure mechanism. This mechanism was not

observed again when the layer thickness was changed back to the previous value.

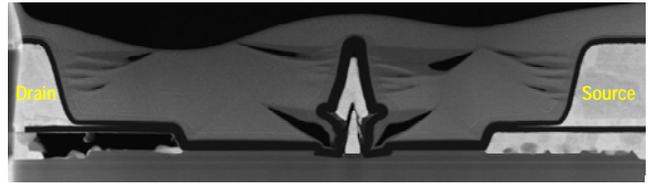


Figure 8. STEM cross-section of drain to source region showing extensive loss of ohmic metal.

#### LONG-TERM, LOW-TEMPERATURE TESTING

An additional test, not currently referred to in existing standards, is an extended test (1 to 2 years) at moderate thermal acceleration over maximum use conditions. This moderate thermal acceleration identifies failure mechanisms potentially masked in high temperature testing. This is shown conceptually in Figure 9. This testing is conducted on both parts during the development phase and on those regularly sampled from the production line. It thus provides information over an extended part of the technologies life cycle.

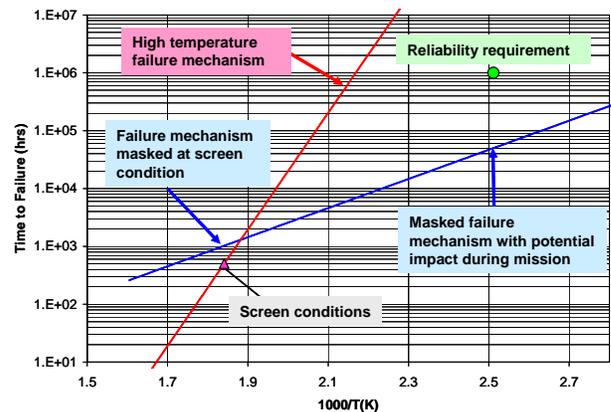


Figure 9. Inability to observe potential low-activation energy failure mechanism from high-temperature testing only.

For GaAs HEMT, results of this testing are shown in Figure 10. The moderate thermal acceleration used was a  $T_j$  of 195°C. The amplifiers show excellent stability and provide confidence in the inherent reliability of the technology.

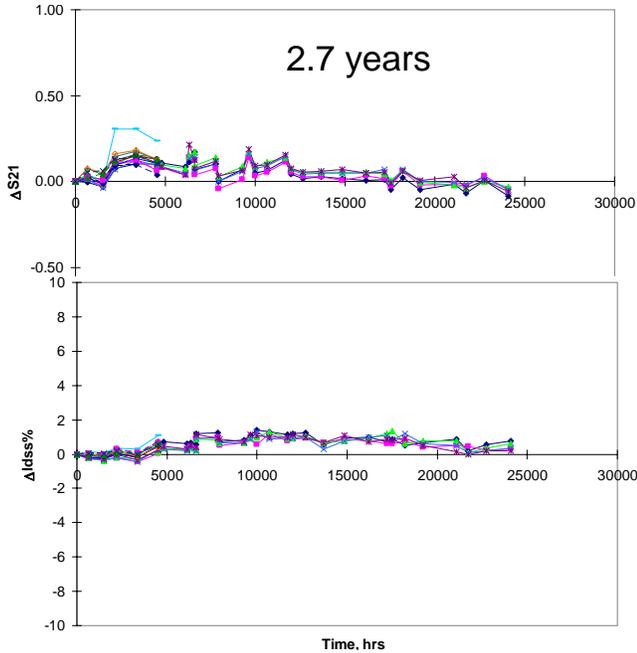


Figure 10. Representative long-term, low-temperature results for 0.15  $\mu\text{m}$  GaAs HEMT technology.

#### SUMMARY AND CONCLUSION

Key components of a comprehensive MMIC reliability approach include multi-temperature and other accelerated life testing; determination of failure mechanisms using both device parametric changes and destructive physical analysis; investigation of anomalous behavior or unexpected failures; and the use of long-term, low-temperature testing. We believe this approach robustly addresses the challenges involved in qualifying MMIC technologies for high-reliability applications

#### REFERENCES

- [1] Yeong-Chang Chou et al., *Hot Carrier Effect on Power Performance in GaAs PHEMT MMIC Power Amplifiers*, Microwave Symposium Digest, 2005 IEEE MTT-S International, pp. 165-168, June 2005.
- [2] Y.C. Chou et al., *Physical Identification of Gate Metal Interdiffusion in GaAs PHEMTs*, IEEE Electron Device Letters, vol. 25, no. 2, pp. 64-66, February 2004.

#### ACRONYMS

HEMT: High Electron Mobility Transistor  
 MMIC: Monolithic Microwave Integrated Circuit  
 NGST: Northrop Grumman Space Technology  
 STEM: Scanning Transmission Electron Microscopy