Layout Design Rule Effects on Capacitor Reliability

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Abstract

A test mask was constructed to evaluate the capacitor layout design rules and their affect on the capacitor yield and reliability. This detailed study, evaluating capacitor design spacings as well as dielectric thickness shows that even perceived large spacings of 2-5 um in the overlay of top and bottom plate metals have a significant effect on capacitor lifetime and reliability.

INTRODUCTION

Prior work on capacitor reliability has focused on dielectric reliability and defects in the dielectric. In this study the physical dimensions of the capacitor in terms of design rules, inter-layer spacings and dielectric thickness are evaluated to determine their effects on yield and lifetime.

TEST RETICLE

A test reticle developed for process characterization, included capacitors of various sizes and shapes, as well as capacitor designs using different layout rules has been previously described.[1] These test devices have been characterized using both ramped and constant voltage test procedures. From that evaluation, the baseline dielectric and capacitor reliability for our process was determined.[2] The test reticle was designed with a series of capacitors with identical capacitance (top plate size 143x143 um), but varying CAD spacing between the several metal layers used in the capacitor construction: capacitor base metal (CB), top plate or overlay metal (OV), air bridge post and bridge. The purpose of these variations was to determine whether the design rule spacing had any affect on capacitor yield or lifetime.

CAPACITOR LAYOUT

For this evaluation a capacitor with an overlay top plate which is fully covered by plated metal was chosen. In that way, any effects of the airbridge plating process would be consistent over the entire capacitor, and the design spacings would apply to all sides and edges of the structure. Design rules for the processes are listed in Table 1, along with the experimental spacings. For lithographic, topological and historical reasons the minimum design spacings are slightly different for the HBT and FET processes.

TABLE 1. CAPACITOR LAYOUT DIMENSIONS
Shaded values are the minimum and maximum values used for the full factorial DOE.

Table 1.		Capacitor Layout Dimensions (um)						
		HBT Min. Design Rule	FET Min. Design Rule	Experimental CAD Spacings (um)				
CB-OV	Overlay inside Cap Base	3.5	2	0.5	1	2	5	12.5
OV-Post	Post inside Overlay	1	2	0.25	0.5	1	2	5.5
Post-Bridge	Post inside Bridge	1	1	0	0.5	1	2	4

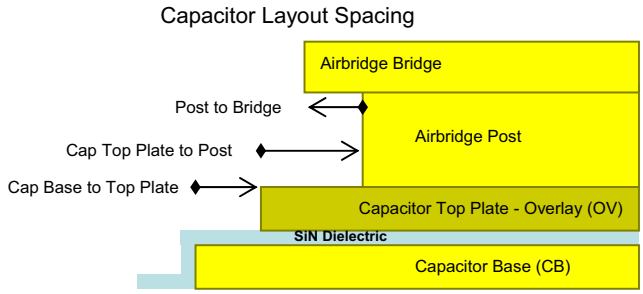

Figure 1. Capacitor layout design rule spacing dimension identification.

The CAD layout spacings were chosen to extend the lithography limits for our design rules to determine whether changes could or should be made. An initial L8, full factorial, experiment was outlined. The design also included a pseudo 'center point'. A selection of capacitors with different spacing values were used to fill out the space allotment of 23 capacitors. An additional 9 capacitors

representing the oldest legacy design were also included in the reticle to be sure the bias voltage effect on lifetime was consistent with our historical results.

The DOE factor settings were chosen to span the layer spacings smaller and larger than the current design rules. Because the variation was expected to be very non-linear, additional factor settings were chosen between the limits of the DOE. These intermediate factor settings were chosen to vary approximately in factors of two. For example, as shown in Table 1, the capacitor base to top plate spacing (CB-OV) factor settings were set at 0.5, 1, 2, 5 and 12.5 um. These values are the mask design spacings. The actual CB-OV spacings on the wafer for the experiment are smaller than the mask design factor settings by 0.5 um i.e. actually, 0.0, 0.5, 1.5, 4.5, and 12.0 um. To complete the experiment, multiple wafers were processed with one of three SiN dielectric thicknesses: 160, 100, and 50 nm.

CONSTANT VOLTAGE TESTING

Previous capacitor testing has shown that either ramped or constant voltage testing may be used for the evaluation of dielectric reliability, and that both methods give essentially equivalent results [2]. For this analysis, constant voltage testing was selected since the maximum lifetime had been previously characterized and was well known. This allowed selection of voltages and total test times consistent with equipment availability. For this study, testing was completed during the off shift so the voltage (electric field) was chosen to allow testing in a single shift overnight test. Capacitors designed to our standard foundry design rules with 160 nm SiN dielectric have a median lifetime of about two minutes when tested using a constant voltage of 146 V (Electric field=0.91 MV/mm). This electric field was utilized to test two capacitors at a time from each of the 104 reticles on a standard in-process wafer probe system overnight. Testing followed a modification of JEDEC and SEMI procedures[3] Capacitance was measured first for each capacitor to determine functional yield. Appropriate bias was then applied with failure determined by capacitor current. After failure, capacitance was measured again to further verify the failure.

YIELD

Fabrication yield for all versions of the design rules for capacitors was essentially 100%. The only capacitors shorted upon initial testing were those few which were visibly damaged. This was somewhat unexpected since the smallest CAD spacing for CB-OV of 0.5 um essentially aligns the edges of the top and bottom plates on top of each other. Any excess metal or 'wing' was expected to be a potential cause for failure.

LIFETIME

Lifetime results from capacitors fabricated utilizing 160 nm dielectric thickness are shown in Figure 2 and capacitors with 50 nm dielectric in Figure 3.[i] Three groups of data are readily apparent in the figures. The groupings correspond to the spacing between the capacitor base and the top plate metal (CB-OV). For all three dielectric thicknesses the same effect was observed: CB-OV separation has the only significant effect on the capacitor lifetime. Three general groupings of data are shown which correspond to the CB-OV spacings of 0.5, 1 um and the combined group 2, 5, and 12.5 um which are nearly indistinguishable. Evaluation of the other factors, OV-Post and Post-Bridge spacing do not show any significant effect on lifetime.

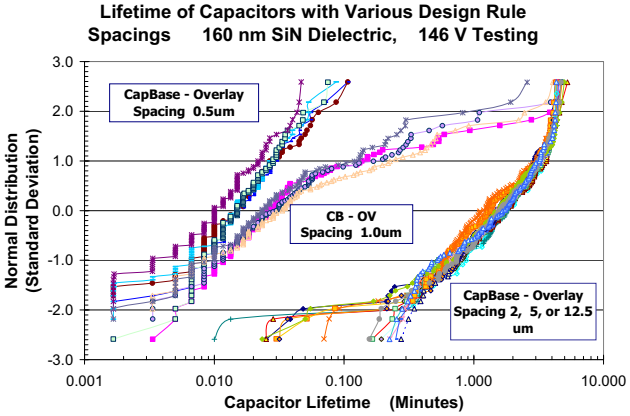

Figure 2. Lifetime results from capacitors fabricated utilizing 160 nm dielectric thickness. Discrete steps in the distribution for short lifetimes result from the 0.1 sec resolution chosen for the test program.

The capacitor base to top plate spacing (CB-OV) of 1um or less results in a median lifetime more than two orders of magnitude less than for spacing of 2 um or more. The spacings of 2 um and larger do not have a statistically significant difference in terms of median lifetime, but the smaller spacing (2 um) has slightly more early failures as can be seen by the spread in lifetime less than -2 standard deviations from the mean. The 2 um spacing data has approximately ~5% compared to <1% early failures for the 5 um spacing.

In Figure 4, the median lifetimes for all capacitor designs are shown for each of the three dielectric thicknesses tested. More than 10,000 capacitors are represented by the data. The median lifetime as a function of CB-OV design spacing for the legacy (12.5 um) down to 2 um show little effect of

[i] Lifetime for the 100 nm dielectric tested at 86 V shows the same variation and distribution as the 160 nm and 50 nm dielectric but is not shown for space considerations.

the design rule spacing on reliability. Below 2 um (1 and 0.5 um CB-OV spacing) the lifetime abruptly decreases by two orders of magnitude.

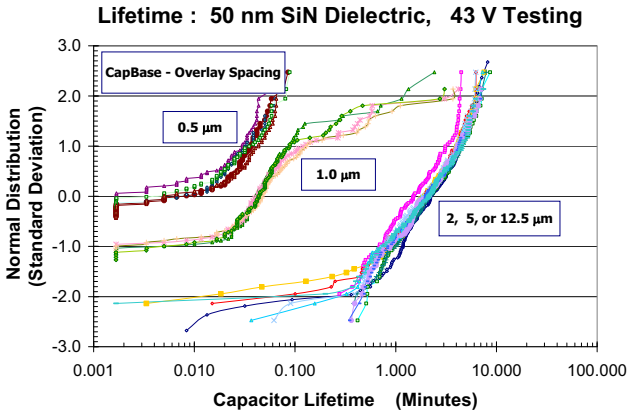

Figure 3. Lifetime results from capacitors fabricated utilizing 50 nm dielectric thickness.

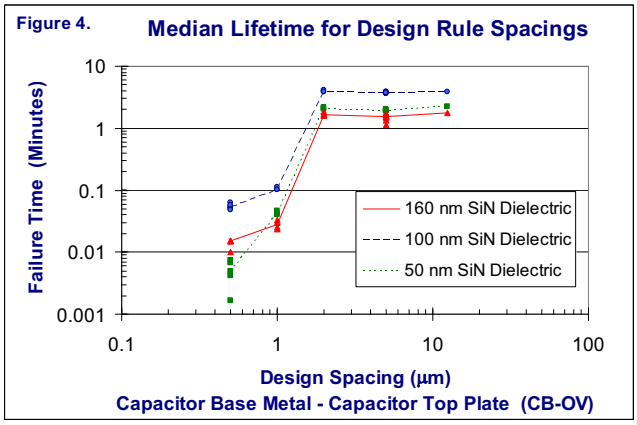

Figure 4. Capacitor median lifetime for the range of design rule spacings. Each of the nitride thickness shows a similar trend with reduced lifetime below 2 um. The difference in lifetime for the different nitride thickness result from slight differences in applied electric field, in thickness from the nominal, and in the roughness of the base metal which acts as a linear subtraction from the nitride thickness.

No difference in capacitance value of devices with different spacings was observed. For the 160 nm dielectric the capacitance mean was 7.1 pF, and standard deviation 1.1%. For thinner dielectrics and larger capacitors (larger capacitance) the standard deviation decreased. This is a result of the inaccuracies of attempting to accurately measure hundredths of a picofarad on automated test equipment.

VISUAL INSPECTION OF FAILURES

Inspection of the failure location revealed an overwhelming number of edge failures rather than interior to the capacitor. This is true whether or not the top plate is partially or fully plated. Edge failures were the predominant failure location for all of the various layout spacings used and the standard capacitors. Figure 5 shows an example of one of the failed capacitors with splatter visible on the contact to the capacitor base metal. Figure 6 is a histogram of the failure locations sorted by the CB-OV spacing. CB-OV spacings of 2 and 5 um have similar distributions. Two particular failures do stand out. The 0.5 um CB-OV spacing has predominant failures on the inner corner where the CB pad connects (Right CBIC). This capacitor base connection pad (CBP) also has a higher percentage of failures in the other spacings considering the relative size of the pad. The physical mechanism for this is not understood, but may be an effect of the proximity of the capacitor to the pad used for automated probe.

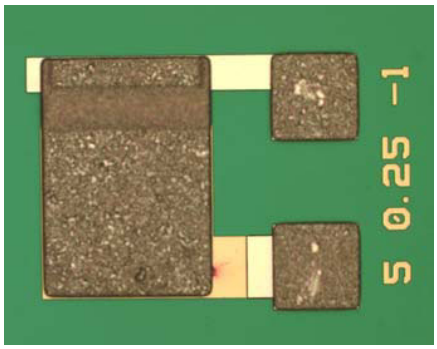

Figure 5. Photograph of one the capacitors tested. Note the splatter on the lower contact pad as evidence of failure. The layer spacings are coded on the right side CB-OV=5 um, OV-Post=0.25 um, and Post-Bridge=1 um. The top plate is fully plated and the airbridge connects to the pad in the top of the photo.

Capacitor corners have a small and relatively consistent failure percentage over the distribution of failure locations. The one other item that stands out is that the 1um spacing has a preponderance of failures on the left side, different from the others. This possibly may result from the slight alignment offset (measured <0.1 um) in that direction on the wafer.

Inspection of the wafers with thinner dielectrics was much more difficult. The lower voltages and hence lower power for the failure (43V for 50 nm and 86V for 100 nm compared to 146V for the 160 nm dielectric) did not leave easily identifiable splatter to indicate failure. Under high magnification inspection, the failure splatter was visible but

inspection of more than a small sample was too time consuming to be feasible.

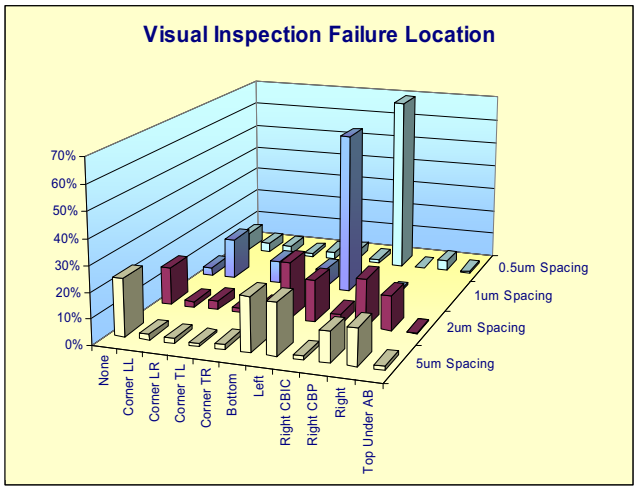

Figure 6. Failure locations of the 4000 capacitors from a wafer with 160 nm SiN dielectric.

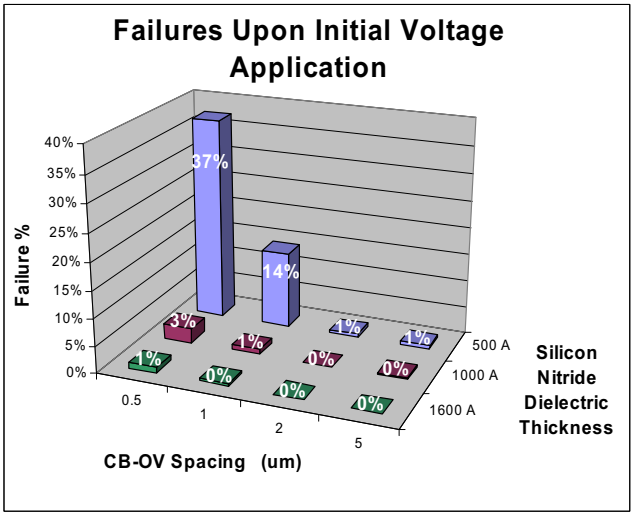

Figure 7 Early Failures. Capacitors that were initially functional but failed in the first 0.2 sec of voltage application.

Failures on initial voltage application are identified in Figure 7. For this chart capacitors that were functional for the initial capacitance measurement but failed in the first 0.2 seconds of voltage application are tallied. For the larger CB-OV spacings of 2 and 5 um, and for dielectric thickness > 100 nm the number of failures is <0.5%. The smallest spacing (CB-OV=0.5 um) and thinnest dielectric (50 nm) have the predominant number of failures, approaching 40%. This high percentage of early failures implies that there are defects associated with the smaller spacings. These are believed to be metal edges and wings associated with the liftoff processes which only have an effect for small spacing and thin dielectrics.

SUMMARY AND CONCLUSION

Constant voltage testing capacitor failure data for more than 10,000 capacitors of different design rule spacing was evaluated for yield and reliability. Failures are predominately located or associated with the capacitor edge, indicating an absence of dielectric defects and indicating the failures are related to the design and lithography. Design spacings do not affect initial capacitor yield, but have a great effect on the lifetime. The capacitor base metal to capacitor top plate spacing (CB-OV) is the only spacing found to have a significant effect on the reliability and lifetime. Design spacings of 1 um and less show increased early failures and more than 2 orders of magnitude shorter lifetime. CB-OV spacings 2 um and larger have equivalent median lifetime but the 2 um spacing may have a slightly increased early failure rate.

ACKNOWLEDGEMENTS

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ACRONYMS

CAD: Computer Aided Design
CB-OV: Spacing between capacitor base metal and top plate or overlay metal.
DOE; Statistically designed experiments
L8: Taguchi nomenclature for a full factorial experiment using 3 factors with 2 settings each: 2^3=8 runs.

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