

# Measuring Liftoff Quality and Reliability with Special Test Structures

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## ABSTRACT:

This work attempts to bridge the gap between manufacturability, quality, and reliability. The investigation is focused specifically on early life failures – the ones that customers actually experience. Focus on defect type failures is necessary to improve reliability on any maturing process. This work supports the notion that quality is an integral part of device reliability. This research advances the knowledge of manufacturability by showing the importance of the relationship between clever layout of test structures, application of ramp stress voltages, finding resulting yield, conversion to quality per units of periphery, and reliability prediction to draw the focus back to what causes failures.

## INTRODUCTION:

Compound semiconductor manufacturing processes will typically utilize metallization patterning techniques called “liftoff.” In addition to being a unique construction procedure, liftoff is also a challenging photolithographic method. The quality of liftoff is commonly evaluated subjectively by inspection: either optically or by use of a scanning electron microscope. This study offers an alternate method of measuring liftoff quality by using specially designed structures that can be measured electrically. These measurements are not only objective and quantitative, but they can be highly automated.

Liftoff is a metal deposition technique that does not include specific metal etching requirements. The process involves the following basic steps, which are depicted graphically in Figure 1:

- A. Apply photoresist.
- B. Pattern photoresist to define x and y dimensions of the metal.
- C. Deposit the metal. Note that the metal covers everything: the remaining photoresist and the patterned areas where the photoresist was removed.
- D. Remove the photoresist, and “liftoff” the unwanted metal on top of the photoresist. Metal remains in the patterned areas.

The metallizations most commonly patterned by liftoff are:

- i) Contacts: gate, source, drain, emitter, base, collector; and ohmic,
- ii) Interconnect: deposited traces which are primarily gold layers;
- iii) Electrodes: top and/or bottom plates of capacitors; and
- iv) Resistors: usually thin film type such as tantalum or NiCr.

Liftoff can be contrasted to the silicon-typical process of depositing a blanket metal, applying photoresist, developing the photoresist as an etch mask, and then “subtracting” the unwanted metal by etching the entire field except areas protected by the photoresist etch mask. Both techniques have benefits and issues, but because of the difficulties of etching gold, the liftoff technique is very commonly used for the gold-based metallizations utilized in compound semiconductors.

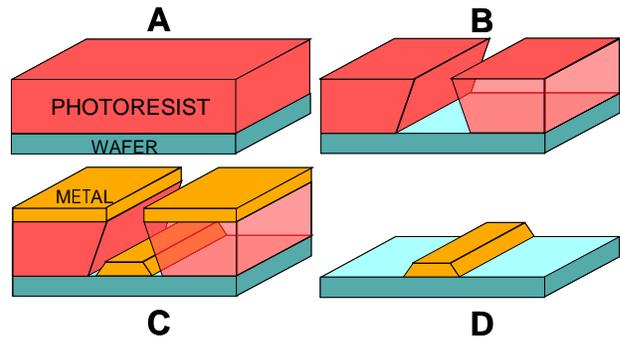


FIGURE 1. BASIC MANUFACTURING STEPS OF LIFTOFF PATTERNING.

## MEASURING LIFTOFF DEFECTS.

Liftoff defects are introduced by excessive process or material variation, random contamination, or mechanical damage during handling. As an example, photolithography defects may cause electrical “near opens” or “near shorts.” The “near shorts” are more prevalent for liftoff on compound semiconductors, and they are accelerated by electric fields resulting in dielectric breakdown between contacts or metal traces. Liftoff shorts were among the first process defects experienced by compound semiconductor customers. Figure 2 shows field return example from 1992.

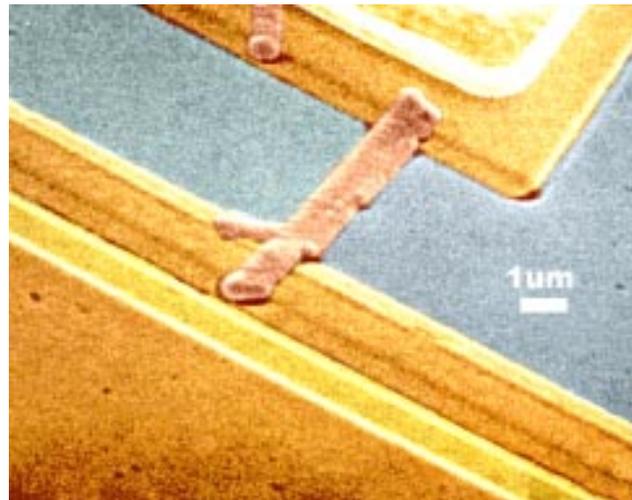


FIGURE 2.

LIFTOFF DEFECT FILAMENT CAUSING AN ACTUAL FIELD FAILURE.

## STRUCTURES

Special structures; including “combs,” “gaps,” “meanders,” and “scales” can be used to measure defectivity in liftoff layers.

A comb is a set of interdigitated fingers as shown in Figure 3. The fingers can be various widths, but the spacing between fingers is normally kept constant. A comb is efficient for measuring large periphery to check for any shorting type defects. Normally, there will be very high resistance (low leakage) between the electrodes until a defect is encountered.

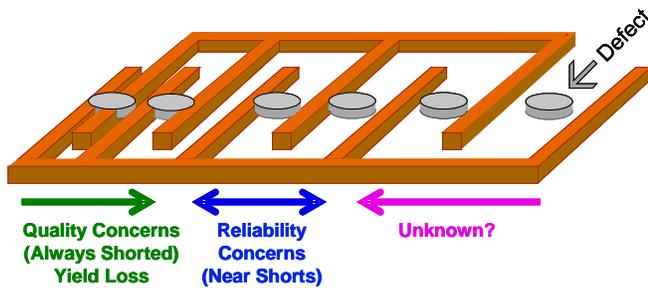


FIGURE 3. SHORTING TYPE DEFECTS FOR LIFTOFF METAL LINES. COMB STRUCTURE WITH CONSTANT DEFECT AND INCREASING SPACE.

Figure 3 shows a simple example of test structure designed to detect intralayer shorting defects. In this case, the size dimensions of the metal and the defect remain constant. As the space between metal lines increases, the defects have different consequences. With the narrowest spacing, the presence of this defect will result in an electrical short. At moderate spacing, the shorts are less probable, but the reliability may be impacted. At the widest spacing, this single defect does not matter. Of course, changes in defect size and frequency of occurrence are significant factors. Various sizes of interconnect fingers and orientation may have a second order effect.

A gap is a field of metal with a space between. Figure 4 shows a typical gap style structure. These shapes are intended to exacerbate defects in areas of larger remaining metal such as for capacitor electrodes, but still include a fair amount of periphery.

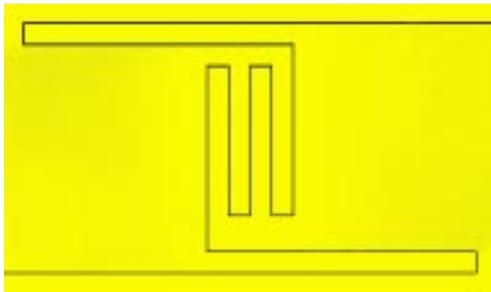


FIGURE 4. BASIC EXAMPLE OF A "GAP" TEST STRUCTURE LAYOUT. LARGE METAL AREAS ARE FOR SUBSEQUENT BOND PAD CONNECTIONS. GAP IS THE UNIFORM DARK LINE AT THE SPACING OF INTEREST.

A meander is a pair of adjacent fingers which fold back and forth against each other. Meanders are a special type of comb structure that can also be used to check for continuity along the length of each meandering electrode. Meanders are very area efficient at maximizing periphery. However, as the periphery is increased (by making the meanders longer) the ability to check for shorts will decrease. The continuity checking can be enhanced by Kelvin sensing the meander lines from both ends.

The most complex structure mentioned in this study is the "Scale." Scaling structures are simply described as a series of combs that are connected in parallel. The feature of interest, such as comb spacing, can be varied across the structures in parallel.

To enhance the interaction of the parallel structures, additional scaling resistors can be added. By placing structures and weighting them with additional resistance, a single resistance measurement can indicate shorting that occurs in combinations of the parallel combs.

#### IMPORTANCE OF USING THE RIGHT ELECTRICAL STRESS

In addition to the physical design of special test structures, the electrical test method is important. Naturally, a selection of voltage and current measurements is an important first step. However, the defects present within various test structures have a wide variation of electrical properties that make them elusive. For example, what is the appropriate voltage for measuring defects? The answer is: it depends. Each type of liftoff layer will have different characteristics as shown in Figure 5.

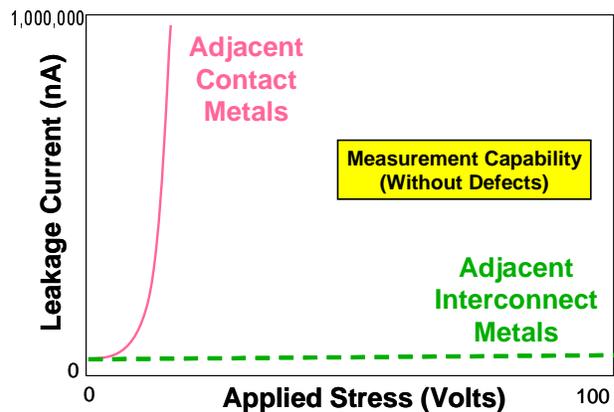


FIGURE 5. RELATIVE DIFFERENCES IN LEAKAGE BETWEEN COMB OR GAP STRUCTURES CONSTRUCTED FROM TRANSISTOR CONTACTS FORMED ON THE SEMICONDUCTOR COMPARED TO INTERCONNECT METALS THAT LAY BETWEEN DIELECTRICS.

Figure 5 shows that contact metals must be limited to low voltage measurements compared to interconnect metals. Adjacent contacts will have inherent leakage that overwhelms any leakage that a defect would contribute. On the other hand, the interconnect metal is typically separated from the substrate, so the applied voltage can be much higher and still discern any contribution by defects.

Application of a high voltage may cause "healing" or "clearing" of many types of liftoff defects. Figure 6 shows an example of this aspect. Figure 6 shows that most test voltages would be ineffective at detecting this particular defect. At all applied voltages up to 10 volts, there is no indication of a defect. Likewise, voltages above 11 volts look perfectly normal. In fact, even the defect (obvious between 10 and 11 volts) was "cured" by the time 11.5 Volts was applied so even a full sweep retest would show no anomalies after the defect has been effectively healed in the initial sweep shown. Figure 6 is an example of lower voltage measurement applied to a gate metal, contact style, comb. This same phenomenon has been observed on interconnect combs as well. Figure 7 shows the distribution of detection voltages for all defects measured in an interconnect style comb between 0 and 100 Volts. Upon examination of the results shown in Figure 7, one would be hard pressed to pick any particular voltage that is singularly appropriate to detect defects over this range.

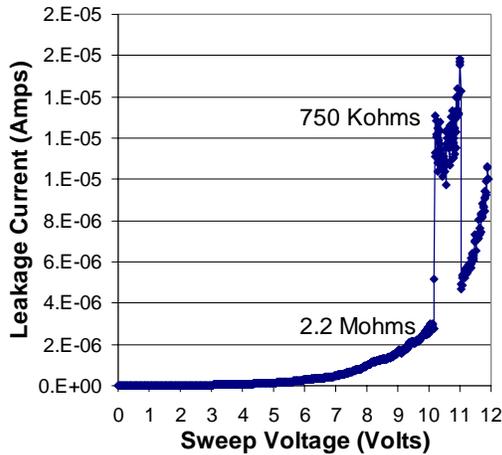


FIGURE 6. RESULTING CURRENT WHEN A GATE COMB STRUCTURE IS SWEEPED UP TO 12 VOLTS. THE LIFTOFF ANOMALY WAS DETECTABLE AS AN INTERMITTANT LEAKAGE BETWEEN 10 AND 11 VOLTS.

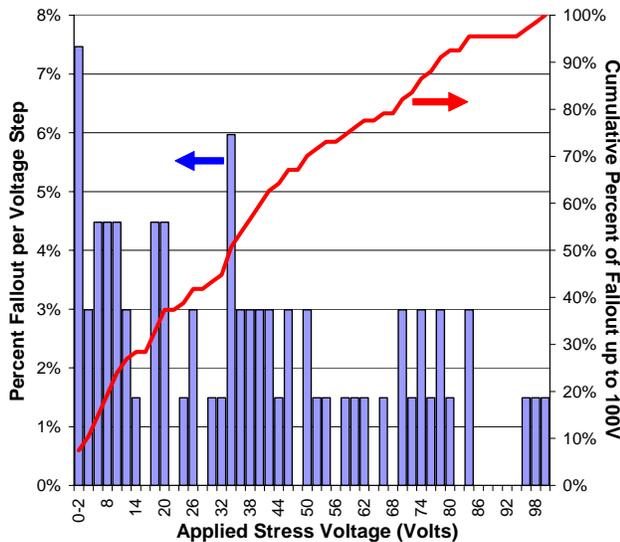


FIGURE 7. DISTRIBUTION OF LIFTOFF DEFECT FALLOUT FOR INTERCONNECT STRUCTURES SUBJECT TO STRESSES BELOW 100 VOLTS.

#### STRUCTURE DESIGN AND DEFECT AMPLIFICATION

In particular, the physical shapes and sizes of comb features were varied in order to exacerbate liftoff difficulty and defect generation during this study of liftoff quality. Figure 8 shows some example results for various orientations and spacings between test structures. This data was collected for a simple, 1 Volt, test measurement on a small sample size of identical test structures. Leakage above a nominal level was considered a defect, and the results are shown in terms of yield (or quality) per this simple measurement.

Figure 8 provides the first important clue towards accelerating the detection of defects: narrow spaces generate more fallout. In Figure 8, we expect very high quality at the minimum allowed spacing layout limit (2um). Eventually, with enough peripheries between the lines, there will be a defect. Assuming there is a practical limit to the periphery, and a limitation to the size of a PCM, another means of acceleration or amplification is sought. In order to increase the likelihood of detecting the rare defects, we propose a decrease in the spacing as an amplifier of defects.

With decreased spacing, more and more defects can be detected, but there is a risk the type of defect will change. For example, smaller and smaller defects will show up with narrowed spacing. These smaller defects may not ever be a concern for wide (nominal) spaced lines. Normally, the size of the defect and the location of the defect relative to metal patterns are the most important considerations. However, we have found that the applied voltage of the quality measurement is equally as important. Fig. 8 shows the liftoff “cliff” is between 0.6-0.9um.

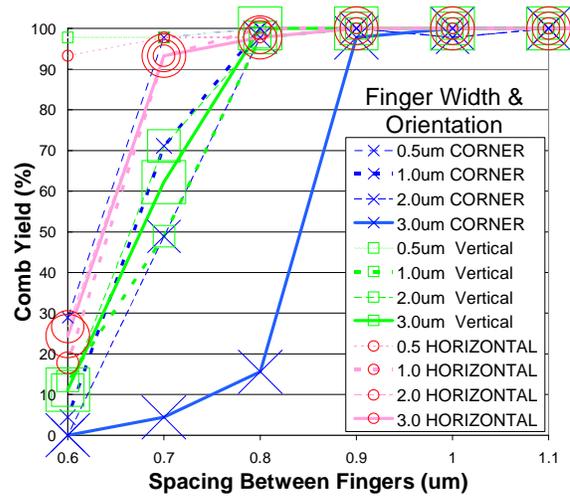


FIGURE 8. INITIAL YIELD LOSS ON 12 TYPES OF COMB STRUCTURES OVER A RANGE OF SIX SPACINGS BETWEEN COMB FINGERS.

Figure 7 shows the second similar clue: higher voltage generates more fallout. A relationship between physical space and applied voltage is intuitive since decreasing space is effectively increasing the electric field – at least for the defects that are nearly, but not yet, shorted in the gap of interest. The use of various spacings in the test structure is how the defects can be “amplified.”[1] The secondary effects of layout orientation (horizontal & vertical) and of the finger width in Figure 8 are noticeable but minor compared to the spacing between fingers. The amplification effect of spacing can be distinguished even further by testing one type layout, with different spacings, over a wide range of applied voltages. The result of this type of examination is shown in Figure 9.

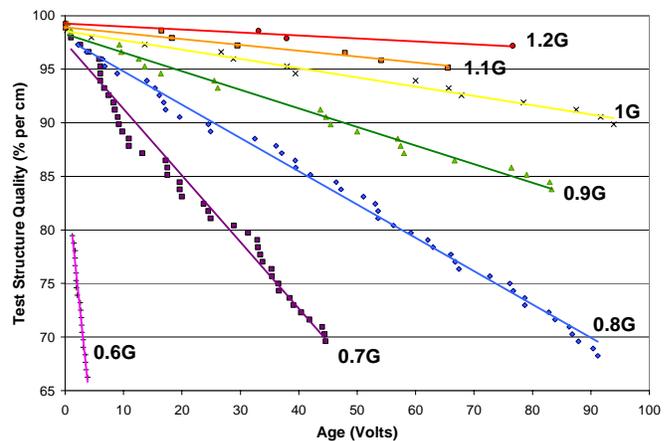


FIGURE 9. QUALITY VERSUS VOLTAGE FOR VARIOUS NORMALIZED SPACINGS LIFTOFF TEST STRUCTURES.

Using the spacing in Figure 9 as a variable, the dependence of quality can be characterized for various spaces between metal traces. Figure 10 shows how quality is affected by the spacing. Figure 10 could obviously be utilized to set layout design rules for optimum quality at a particular periphery (1 centimeter in this example). However, we will exploit our knowledge of this curve to “amplify” detection of defects for populations which follow this relationship. If our total periphery was 1 centimeter, we would expect to achieve 100% yield at spacings wider than 1.4um between liftoff features. However, we can also utilize the voltage aspect from Figure 9 to further enhance our predictive capability. Figure 11 shows how the defectivity is impacted by spacing on a volt\*centimeter basis.

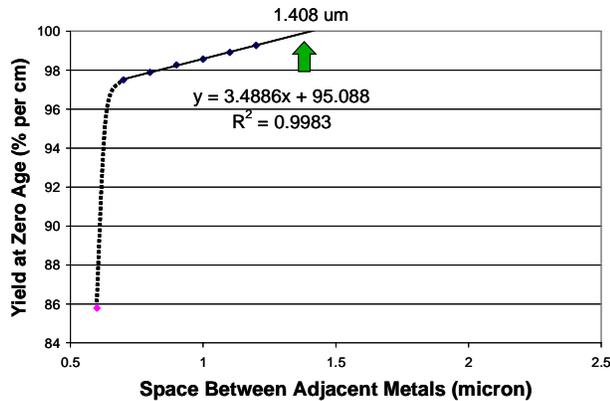


FIGURE 10. QUALITY VERSUS SPACING FOR A 1CENTIMETER PERIPHERY BETWEEN INTERCONNECTS.

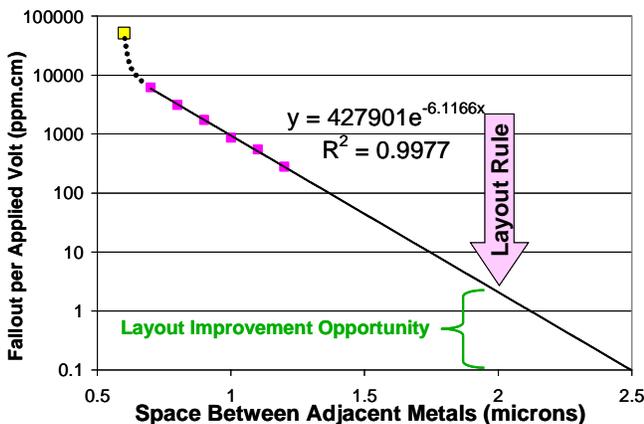


FIGURE 11. PREDICTED DEFECTIVITY IN PARTS PER MILLION PER CENTIMETER PER VOLT.

The use of voltage stress was found to have particularly interesting reliability results. By applying a spectrum of voltages to various experimental structures, results similar those reported for reliability stressing of MIM capacitors were obtained. The relationships of voltage and time relative to reliability are just as interesting for our special liftoff structures as they are for capacitors. To illustrate, please see Figure 12. Here are two populations of test structures stressed up to ten volts. The defectivity is similar for the first 2 volts. At the 2 Volt stage of the ramp, one population is held for 1 hour at 2 Volts while the other population continues its ramp uninterrupted. During the hour long 2V lifetest, 5 failures occurred. This example shows that one hour at 2 Volts is roughly equivalent to 2 Volts of ramp. A simple relationship of time and voltage is shown empirically. This is why the x-axis is labeled as “Age” in Figure 9.

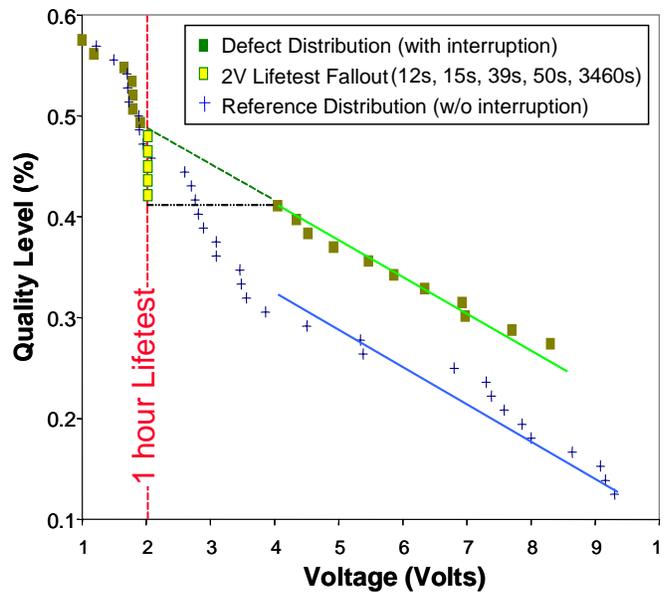


FIGURE 12. DEFECT DISTRIBUTIONS VERSUS VOLTAGE FOR A CONTROL POPULATION AND ONE WITH A 3600 SECOND, 2V LIFETEST INSERTED.

#### SUMMARY

As a result of using the special test structures and electrical measurement techniques described here, manufacturing technology can be improved because:

- 1) Structures capable of detecting liftoff anomalies by simple electrical measurements have been described.
- 2) The dimension of physical space between metal electrodes has been demonstrated as an amplifier of defect detection.
- 3) Voltage can be combined with physical amplification to further accelerate defect measurements as alternatives to increasing areas and peripheries of monitor structures.
- 4) A similarity between metal shorting defects caused by liftoff and extrinsic capacitor defects is presented.
- 5) Voltage and time were found to be roughly interchangeable in their ability to accelerate reliability failures.

These results have unveiled the ability to measure liftoff defects and apply improvement techniques that have been established for other structures – such as capacitors. This opens opportunities for measuring, monitoring, and screening in space efficient ways not previously discussed for liftoff defects occurring during manufacture of compound semiconductor devices.

#### REFERENCE

1. W.J. Roesch and D.J.M. Hamada, “Studying Yield and Reliability Relationships for Metal Defects,” Proceedings of the 2004 ROCS Workshop, Oct.24, 2003, Monterey, CA

#### ACRONYMS

- DPM: Defects Per Million
- NiCr: Nickel Chrome or nichrome
- MIM: Metal Insulator Metal
- PCM: Process Control Module
- PPM: Parts Per Million
- ROCS: Reliability Of Compound Semiconductor