Analysis of DC-RF Dispersion in AlGaN/GaN HFETs using RF Waveform Engineering

Chris Roff, [1] Johannes Benedikt[1] and Paul J. Tasker[1]
D.J. Wallis, [2] K.P. Hilton, [2] J.O. Maclean, [2] D.G. Hayes, [2] M. J. Uren[1,2] and T. Martin[2]

[1]Cardiff School of Engineering, Cardiff University, Cardiff, UK. email: roffc@cf.ac.uk
[2] QinetiQ Ltd., Malvern, Worcestershire, UK. WR14 3PS

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Abstract

This paper describes an observed difference in how DC-RF dispersion manifests itself in AlGaN/GaN HFETs when the devices are driven into different RF load impedances. The localised nature of the dispersion on the IV plane has been observed in RF waveform measurements and is explained through physical modelling. The difference in dispersive behaviours has been attributed to the geometry of the trap induced virtual gate region and the resulting carrier velocity saturation being overcome by punch through effects under high electric fields.

Introduction

GaN HFETs are an ideal technology for radio frequency power amplifier applications due to their good thermal performance and their capabilities for high frequency and high power operation [1][2]. However, GaN HFETs have been known to suffer from trapping problems resulting in DC-RF dispersion - a phenomena also described as "current slump" or "knee-walkout" - which limits the power capabilities of these devices [3].

The general belief is that the measured dispersion in GaN HFET structures is caused by electron leakage from the gate onto the semiconductor surface on the drain side of the device [4], a process exacerbated by the high operational drain bias voltages in many GaN applications. This leakage is believed to lead to the "virtual gate" effect, whereby the electrons accumulated along the surface generate an electrostatic charge which acts to partially deplete the conducting channel [5]. The end result of which is that less current is available in the active channel and therefore RF output power is reduced.

This work presents an analysis of dispersion effects seen in 2x100µm wide AlGaN/GaN HFETs grown on a 4H SiC substrate, with a 0.25µm gate length and an approximately 4µm source-drain gap [6]. The RF performance of the devices in a variety of RF load configurations has been investigated using the time domain RF waveform measurement systems at Cardiff University. Additionally, physical modelling simulations have been conducted using Silvaco Atlas in order to draw conclusions about the device behaviour.

Measurement Setup

Waveform measurements were performed on 2x125µm AlGaN/GaN HFETs measured on-wafer using the time-domain measurement system with active harmonic load-pull shown in Figure 1. The waveform measurement system operates using an Agilent 70820A Microwave Transition Analyser (MTA) with vector correction, which allows input and output voltage waveforms to be sampled. A sweeper at the source provides input power at the fundamental frequency (900MHz for all measurements in this paper). An active harmonic load-pull system is used to present the device with a range of loads. RF probes are used to allow on-wafer measurements, and the whole system is computer controlled [7].

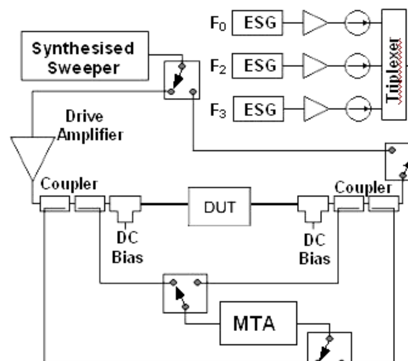

Figure 1 – Schematic of the waveform measurement system

Measurement Results

The DC-RF dispersion can be readily observed in pulsed-IV and RF waveform measurements made at different static drain biases. It is believed that more electrons become trapped in surface states as the drain bias increases, resulting in more dispersion. This can be seen in Figure 2 where RF dynamic load-lines measured at 900MHz are shown for four different drain biases and a range of fundamental load impedances – a technique we have termed

a 'fan'-diagram [8]. The dynamic knee boundary can be seen to shift with the increasing drain bias.

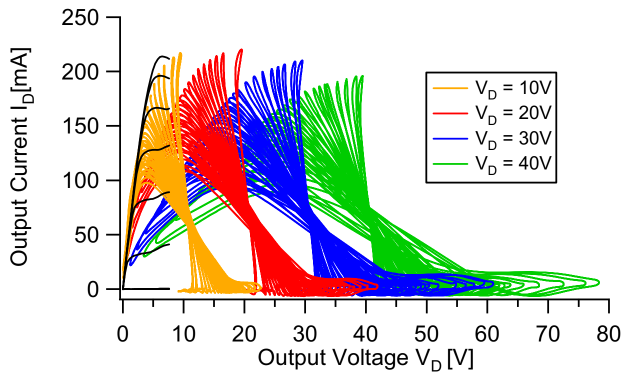

Figure 2 – Measured RF load-line fan diagrams for four Class A bias points, V_D = 10V, 20V, 30V and 40V demonstrating increased dispersion with drain bias. Load-lines are overlaid on DC-IVs measured from V_G = -6 to 0V in 1V steps.

It is possible to observe in Figure 2 that different dispersion behaviours can exist at the same static bias point. Indeed, we can split the IV into three distinct regions where the dispersion is very different. To illustrate these regions the RF boundaries mapped by the fan diagrams have been traced out in Figure 3. Here region (a) describes the low current on-resistance boundary where very little dispersion is seen. Region (b) describes the knee region proper where the dispersion is most pronounced. Finally, region (c) covers the saturation region which shows less dispersion as the drain voltage increases.

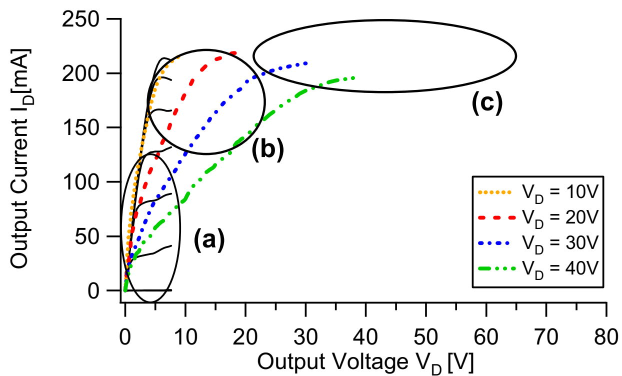

Figure 3 –RF boundary conditions mapped out by the dynamic load-lines of Fig. 2 showing three regions with differing dispersion behaviour.

SIMULATION RESULTS

To understand these measured results physical model simulations were run using Silvaco ATLAS. Firstly the device structure was simulated with no surface trapping effects included. A second simulation was then run to model the effect of trapped charge corresponding to a static class B bias condition. The virtual gate effect has been modelled as a localised distribution of electrons on the surface of the device immediately next to the gate on the drain side. Figure 4 shows the fixed charge distribution used, with a 75nm region of $12x10^{12}cm^2$ charge density placed next to the T-gate to model the electrons trapped in surface states.

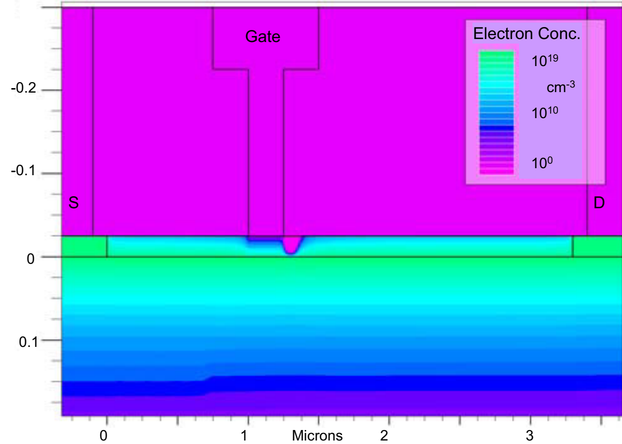

Figure 4 – Contour plot of electron concentration for V_G=0, V_D=0. The reduction in the channel due to the virtual gate can be seen on the drain side of the gate.

Using these two simulations, the virtual gate device model can then be compared with the standard device model to show the effect of localised surface charge on dispersion. Figure 5 shows the comparison IVs of the two simulation cases. The IVs of the standard device can be considered as baseline performance with no trap effects. The case with the surface charge included shows dispersion behaviour that is very similar to the measurement results. The same three distinct regions where different amounts of dispersion occur have been captured by the modelling approach.

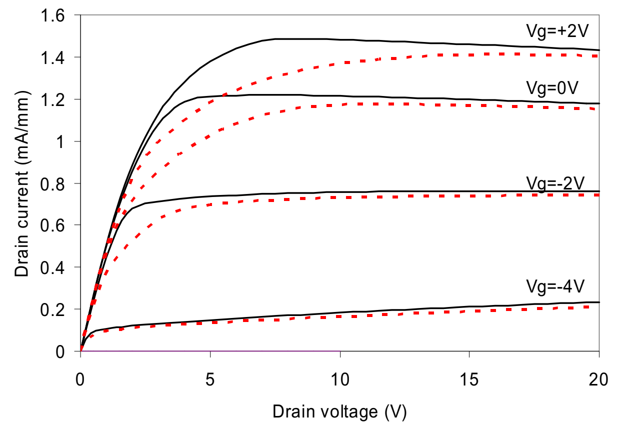

Figure 5 – Simulated IV characteristics for the baseline case with no dispersion (full line) and the virtual gate model (red dashed lines).

DISCUSSION

The surface charge model has reproduced the observations seen in the measured waveform results, suggesting that it has also captured the impact of the trapped charge in the device. The main effect of the small area of surface charge beside the gate is to reduce the amount of charge available in the channel for a small area immediately beneath the virtual gate. This small area of reduced charge results in a limited saturation current in the knee region. However, because the area is geometrically small it has very little effect on the overall resistance of the channel. Furthermore, at high drain voltages punch-through effects (similar to short channel behaviour) occur which allow the current to recover with increasing drain voltage.

This virtual-gate model can now explain the three regions with different dispersive behaviour. Firstly, region (a) where there is very little dispersion with increasing drain bias can be explained because the IV characteristics are dominated by the parasitic access resistance (on-resistance) which is not greatly affected by the small depleted region introduced by the surface charge. Region (b) is where the surface charge has the most significant effect because the channel current saturates prematurely compared to the DC case. Region (c) also suffers from reduced current, but at higher drain voltages the current is able to punch through the small saturated region leading to a gradual recovery of current with increasing drain voltage.

CONCLUSIONS

This paper has presented a clarifying insight into DC-RF dispersion problems in GaN HFETs through RF waveform measurements performed across a range of RF load impedances and physical device modelling. It has been shown that the virtual-gate surface charge created when devices are biased on can explain the different dispersion effects seen when different regions of the device IV are probed by RF signals.

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ACRONYMS

HFET: Heterostructure Field Effect Transistor
MTA: Microwave Transition Analyser