Title: Gallium Nitride Surface Treatment Study for FET Passivation Process Flow Applications

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Abstract

Wet chemical etches were investigated for surface passivation applications of Gallium Nitride grown on c-plane sapphire substrates. Samples were treated and then analyzed utilizing XPS. MISFET structures were fabricated on two Gallium Nitride samples in a split experiment with and without acid treatment prior to gate dielectric deposition. Devices with acid treatment showed decreased gate leakage, increased I_{on}/I_{off} ratio, decreased subthreshold swing, increased pinch off voltage and increased transconductance over those without.

INTRODUCTION

Gallium Nitride (GaN) is currently an active research area with its potential for use as Radio Frequency (RF) and power devices due to high breakdown voltage and thermal dissipation. The GaN HFET has specifically been added to the ITRS roadmap in recent years as a device for RF Wireless applications [1]. In order to increase performance and decrease gate leakage current in GaN FETs for such applications, improved surface passivation processes have been identified as a critical area for development. Silicon Nitride has widely been researched as a passivation layer for GaN FETs [2, 3, 4].

Wet chemical etching can also be used to passivate semiconductor surface [5], however, most GaN wet etch techniques require optical activation [6]. For instance in these etch types, samples may need to be exposed to a UV laser within a chemical bath. Incident photons create electron-hole pairs which facilitate the etching from the semiconductor surface. In this work, a surface treatment using a two-chemical GaN wet etch technique to decrease surface related defects prior to gate insulator deposition was investigated [7]. The etch process sequentially submerses samples in a strong oxidizing reagent, rinsed and then placed in a strong reducing reagent.
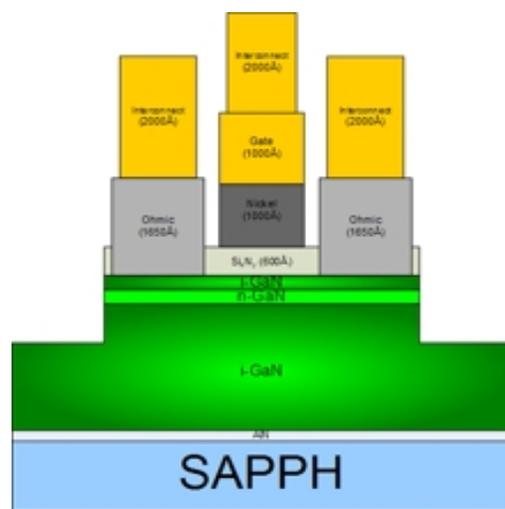
FABRICATION

Devices were fabricated on 0.50μm not-intentionally doped hexagonal-GaN grown on c-plane sapphire substrates by metal-organic chemical vapor deposition (MOCVD). GaN was doped with 0-20nm of either n-type Silicon or p-type Magnesium and capped with a 0-20nm of unintentionally doped GaN. The resulting samples were submersed in either potassium persulfate ($K_2S_2O_8$) or potassium hydroxide (KOH) for 30 seconds and then rinsed in DI Water for 30 seconds [7].
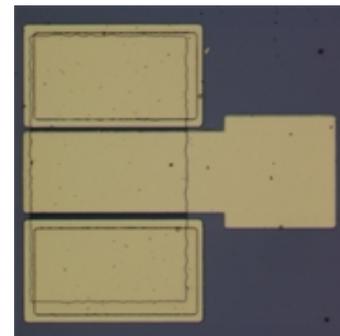
(a)

(b)

Figure 1: (a) top-down microscope image and (b) cross-section of GaN MISFET devices fabricated with gate length L_g=50μm.

The samples were then immediately characterized by X-ray Photoelectron Spectroscopy (XPS) using Riber LAS-3000 with a K_α Mg source for analysis of surface chemical composition. Data was collected at 55° from sample to analyzer, yielding a 20-50nm measurement depth.

The etch process was used in combination with heuristically identified surface-appropriate dielectrics to facilitate surface passivation and investigate leakage current reduction. Several GaN MISFET (Metal Insulator Semiconductor FET) structures were developed in a split experiment: one wafer with $K_2S_2O_8$ treatment before silicon nitride deposition and one without acid treatment before deposition. All other processing steps were identical for both wafers.

Gate dielectric was deposited via PECVD at 300°C with a thickness of 60nm. Titanium/Aluminum/Nickel/Gold (15nm/65nm/35nm/50nm) ohmic contacts were deposited using electron beam deposition and lift-off. Ohmic contracts were subsequently annealed at 850°C for 60 seconds. Device gates were fabricated with Nickel/Gold (100nm/100nm) by electron beam deposition and lift off. Finally, Gold device interconnect pads (200nm) were deposited by electron beam evaporation and lift off. A top-down microscope image of device measured is shown in Figure 1a. Devices are DC MISFETs with gate length L_g = 50μm and gate width W_g = 100μm. A modeled cross-section of the device fabricated is shown in Figure 1b.

SURFACE CHARACTERIZATION

Comparison sets of acid/base samples were analyzed using XPS and AFM. AFM results show an increase in surface roughness, indicating etch induced change in surface morphology [7]. For each sample, a survey XPS scan was use at broad resolution to determine the elemental presence and concentration. The concentrations were semi-quantitatively analyzed with CASAXPS™ bi-numerical signal integration for recognized element signals as an atomic percent. To an accuracy of ~1%, the surface composition was assessed by comparing the N/Ga and O/Ga ratios to correlate acid/base treatment the surface composition or oxidation.

For preferential nitrogen removal then N/Ga ratio should be lower than that found in an unetched control. For an i-GaN with a 0-20nm surface layer of n-GaN (1E19), the base N/Ga ratio decreased by 0.59, while the acid decreased by 1.22, which seems to verify the preferential removal of nitrogen from the surface. However, subsequent studies on similar sample yielded different results, where N/Ga ratio for the sample that underwent a 30 second base etch showed an increase of 0.15 and the 30 second acid treated sample showed an increase of 1.45. When the duration of the treatment was increased to 60 seconds the base ratio

continued to rise and the acid N/Ga ratio decreased below the control by 0.26. We believe that this reverse in N/Ga ratio over time shows that it must be etching through multiple atomic layers as no consistent saturation was observed. The difference between the two control N/Ga ratios was 1.97, which was much larger than any difference seen in the ratios due to treatments. This fact, along with the opposing results when repeated, shows that it cannot definitively be stated that the acid strips the nitrogen at the interface. Similar results for the N/Ga ratio were seen in both the p-GaN and i-GaN samples.

Most of the samples exhibited a decrease in O/Ga ratio when treated with base or acid. The exceptions were one n-GaN treated with acid for 30 seconds, and both i-GaN samples treated with acid for 30 seconds. An increase in this ratio would be beneficial because it would show the presence of a native oxide at the interface that would help in passivation. Again only one data point was outside of the variation in the controls, which means that nothing can definitively be said.

The most useful data that found was that the Ga 2p3/2 peak did show a shift after etching with base or acid. The peak shifted from the normal position of 1118.1eV for the controls to 1117.5eV after treatment. When compared with known data a Ga2O3 peak appears at 1117.4eV [8, 9]. Therefore, it would seem that this treatment does create a native oxide which could lead to beneficial passivation and better electrical data.

ELECTRICAL CHARACTERIZATION

Devices from both wafers were characterized and compared for performance differences. Normalized families of curves of representative measured GaN MISFET devices with and without acid pretreatment are shown in Figure 2. Devices are depletion-mode FETs with pinch off voltage ranging from -8.5 to -6.5V.

TABLE 1
DEVICE PARAMETERS COLLECTED FOR
ACID/NO ACID DEVICES

Sample ID	Subthreshold Swing (mV/dec)	I_{on}/I_{off} Ratio	V_{pinch} (V)	Peak g_m @ V_g = 2V (mS/mm)
Acid01	592	2826	-7.6	0.18
Acid02	1182	191	-6.5	*
Acid03	1062	399	-6.5	*
NoAcid01	2954	42	-8.0	*
NoAcid02	3062	43	-7.8	0.11
NoAcid03	2720	227	-8.5	*

(* denotes value not calculated)

Both devices show normal FET characteristics with satisfactory drain current pinch off. For a common V_{gs}

samples with acid treatment show increased drain current over those without treatment.

A comparison of device gate current at $V_{ds} = 0V$ is shown in Figure 3. The devices with acid treatment show an order of magnitude decrease in gate leakage for negative V_{gs} as compared to those without acid treatment. It is unclear at this time what current transport mechanism shown in this mode of operation. Future measurement utilizing a temperature controlled chuck may differentiate between direct tunneling or trap assisted Fowler-Nordheim tunneling through the gate dielectric.

Table 1 details collected device parameters for samples with and without acid treatment. Samples that received acid before insulator deposition show increased I_{on}-to-I_{off} ratio, decreased subthreshold swing and increased pinch off voltage. When comparing devices with similar pinch off voltage (Acid01 and NoAcid02 in Table 1), devices treated with acid show a decrease of 5 times in subthreshold swing and a increase in I_{on}/I_{off} ratio of more than 65 times over those without acid treatment. A transconductance versus gate voltage comparison is shown in Figure 4. Devices that were treated with acid show an increase in peak transconductance over those without acid treatment. However, treatment with acid showed no significant V_{gs} shift in the location of this transconductance peak.

CONCLUSION

An investigation of the surface chemistry of Gallium Nitride samples grown on c-plane sapphire substrates via XPS was conducted. No conclusive evidence was found as to the selectivity of $K_2S_2O_8$ or KOH for etching Gallium or Nitrogen. However, a shift in the $2p^{3/2}$ Gallium peak suggests the formation of Gallium Oxide at the surface when samples are submersed in $K_2S_2O_8$ or KOH. Also an investigation of a GaN wet etch technique for FET surface passivation was conducted. Devices that were treated with $K_2S_2O_8$ prior to gate dielectric deposition showed decreased gate leakage, increased I_{on}-I_{off} ratio, increased pinch off voltage and increased transconductance.

Future work will include further study of the gate dielectric and subsequent gate leakage. A quantum mechanical investigation of wave function penetration in MISFETs with and without a gallium oxide layer at the GaN surface may yield a better understanding of the gate leakage differences between these devices.

The combination of this acid/base surface treatment and high-κ gate dielectrics has been proposed. GaN FETs with Lanthanum Oxide (La_2O_3), Scandium Oxide (Sc_2O_3) or Hafnium Oxide (HfO_2) may show increased GaN FET gate capacitance and therefore drain current performance.
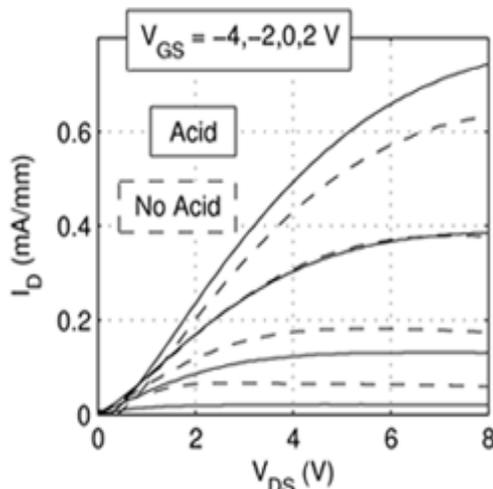

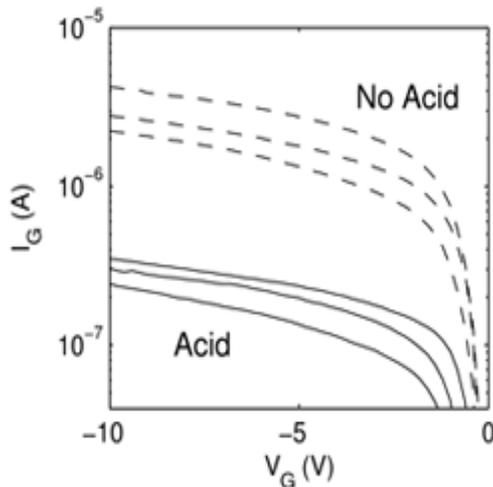**Figure 2:** Representative family of curves of fabricated GaN MISFET devices with and without acid pretreatment.

Figure 3: I_g vs. V_g at $V_{ds} = 0V$, gate leakage comparison of samples with and without acid pretreatment
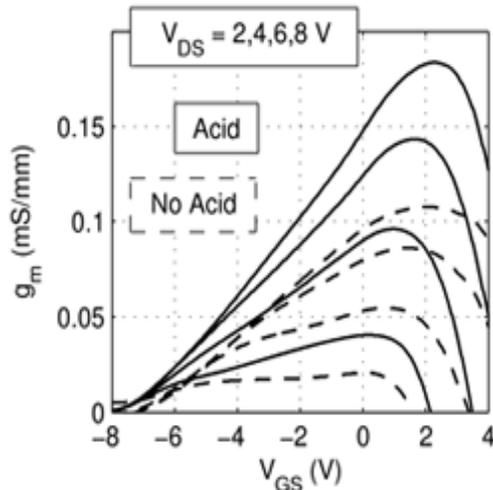

Figure 4: g_m vs. V_g comparison of devices with and without acid pretreatment.

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ACRONYM LIST

FET: Field Effect Transistor
GaN: Gallium Nitride
ITRS: International Technology Roadmap for Semiconductors
MISFET: Metal Insulator Semiconductor Field Effect Transistor
MOSFET: Metal Oxide Semiconductor Field Effect Transistor
MOCVD: Metal Organic Chemical Vapor Deposition
PECVD: Plasma Enhanced Chemical Vapor Deposition
HFET: Heterojunction Field Effect Transistor
RF: Radio Frequency
XPS: X-ray Photoelectron Spectroscopy