GaAs MESFET with Source-Connected Field Plate for High Voltage MMICs

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Abstract

In this paper we show the results of a source-connected field plate development effort for MMIC-compatible planar HV MESFETs. It is shown that best power performance is obtained from this process using devices incorporating both gate-connected and source-connected field plates.

INTRODUCTION

Over the past decade, the maximum operating voltages of microwave transistors based on compound semiconductor technology have been steadily increasing, enabling the design of higher performance electronic systems at lower overall cost. Regardless of the semiconductor material used, field plates are a common feature of high voltage FETs. The specific implementation of a field plate - its geometry, resistivity, dielectric composition and thickness – can have a profound impact on its influence over device operation. Another equally important variable is the connectivity of the field plate – whether it is electrically connected to the gate, the source, or even externally biased as a fourth terminal of the device. Despite numerous reports on various field plate configurations [1-5], remarkably little has been published directly comparing the effects of different field plate configurations [6].

Field plates enhance high voltage operation through multiple mechanisms. One mechanism is the influence on the electric field at the drain edge of the gate electrode. By reducing the field at this location, the off-state gate-drain breakdown is increased. This is exclusively an electrostatic effect; therefore, either source-connected field plate (SCFP) or gate-connected field plate (GCFP) devices should exhibit this improvement. Another mechanism is the mitigation of surface trap effects, resulting in higher RF current in the device. RF modulation of a field plate could have a significant effect upon this mechanism which would represent an advantage for GCFP FETs. Both of the aforementioned mechanisms depend strongly upon the quality of the semiconductor passivation. A third mechanism, not exclusive to high voltage operation, is the influence on FET capacitances. The desired effect is the reduction of gate-drain capacitance through shielding. This is an electrostatic effect clearly not obtainable with a GCFP alone. Of course, the introduction of parasitic MIM capacitance between a SCFP and gate, or the increase in electrical gate length due to the MIS element of a GCFP causes unavoidable detrimental effects from the increase of gate-source capacitance.

Achieving improved device performance with field plates requires careful selection of the field plate variables. While these effects can be evaluated through 2-dimensional device simulation, doing so accurately in a predictive fashion is exceedingly difficult owing principally to uncertainty in the parameters associated with the non-idealities of the materials, especially traps in the GaAs, both in the bulk material and at its surface. This leaves empirical evaluation as the only practical approach. This paper will report on the results of such an investigation into the effects of source- and gate-connected field plates on planar, ion-implanted GaAs MESFETs.

DEVICE STRUCTURE

The high voltage MESFET device technology used in this work is Tyco Electronics' HVMSAG™ process. This process is an extension of 10V MSAG™ power FET technology, based on a refractory metal gate, planar, ion-implanted GaAs MESFET. The HVMSAG™ FET achieves operation up to 28V through optimization of active layer parameters and spacings and gate structure, including a GCFP, as shown in Figure 1. This HV FET has been developed as a robust, highly manufacturable process for fabricating high voltage power MMICs operating at S-band and lower frequencies [7].

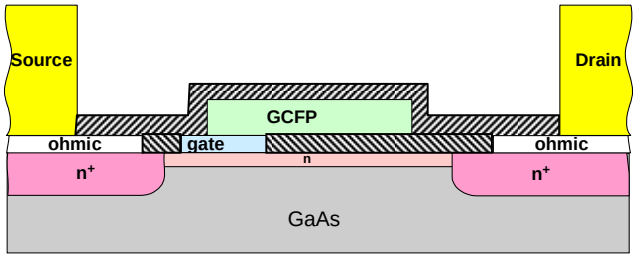

Figure 1. Simplified cross section of the HVMSAG™ gate-connected field plate ion implanted MESFET.

To investigate the possibility of improving performance of the HVMSAG™ FET through the addition of a SCFP as shown in Figure 2., two new mask layers were added to the process flow: a metallization layer for the SCFP electrode and a dielectric glassivation layer for this new metallization to provide environmental protection equivalent to the existing process. In this structure, the MIM capacitor dielectric layer of the existing MMIC process flow serves as the interlevel dielectric isolating the SCFP from the GCFP.

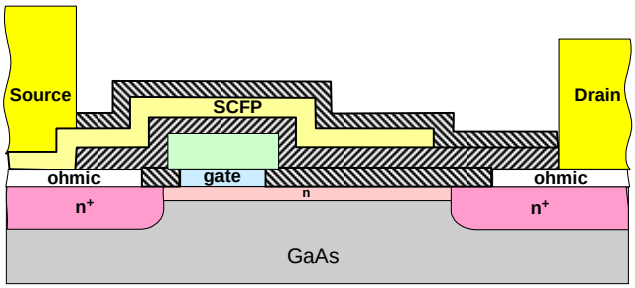

Figure 2. Simplified cross section of a source-connected field plate MESFET as implemented in this work.

Parameter	GCFP	SCFP	T-Gate	Units
I_{peak}	344	345	341	mA/mm
BV_{gdo}	51.2	44.6	46.2	Volts
BV_{ds}	41.1	33.6	33.9	Volts
Pulsed I_{peak}	192	156	113	mA/mm
Gm	38.7	30.3	30.0	mS/mm
Cgs	1405	1487	938	fF/mm
C_{gd}	43.5	11.9	20.7	fF/mm
R_{ds}	549	567	476	Ohm*mm
f_{max}	14.5	21.8	18.7	GHz

Figure 3. dc, pulsed, and RF parameters for FETs with different field plate structures. The quiescent bias for pulsed current measurement is 24V and 10 mA/mm. s-parameters are measured at the same bias.

Device Development

A reticle was designed for process development and device characterization which included standard HVMSAG™ FETs, process characterization structures for the new mask layers, and an array of 256 SCFP FETs representing the full factorial combination of several values for the primary critical dimensions associated with the field plates: the GCFP dimension; the SCFP dimension; the separation between the drain-side implants and SCFP.

The process characterization structures were utilized to develop processes for the new layers suitable for SCFP fabrication. Key characteristics are critical dimension control, metallization step coverage, and dielectric leakage and breakdown. dc and RF characterization established that the processing required for the new layers did not degrade the performance of the FETs

The general approach employed for FET characterization was as follows. dc parameters, s-parameters, and pulsed current were measured on a subset of the SCFP FET array which spanned the full range of the dimensional variables. This was done at multiple reticle sites across each wafer, providing data on more than 250 devices per wafer. From analysis of this data, the most promising devices were selected for large-signal RF characterization. For this purpose, 1.6mm FETs mounted on carriers were tested under 24V bias at 3.8GHz on a Maury load pull station. Small-signal gain and saturated output power were collected under optimum power tune.

Device Characteristics

To examine the effects of field plates unambiguously, the SCFP FET most similar in channel design to the HVMSAG™ FET was selected for comparison. These devices share the same channel implant structure, gate length, and field plate extension past the gate center line. The SCFP FET in this comparison has a conventional T-gate, a structure with minimal overhang past the Schottky contact of equal dimension on both source and drain sides, without what would be considered a GCFP. A third device, identical to the SCFP FET, but omitting the field plate, is included in the comparison to clearly identify the effects of each field plate structure. Several key parameters for these three devices are shown in Figure 3. An examination of the parameters provides insight into the physical behavior of both field plate structures, largely confirming expectations.

dc channel current is independent of device structure, aiding in the comparison among them. The influence of field plate configuration is evident in several parameters. It significantly affects breakdown voltage. The GCFP increases breakdown several volts, but the SCFP has absolutely no effect on it. While this is expected for 2-terminal gate-drain breakdown (BV_{gdo}) where the source electrode is allowed to float electrically, it is initially surprising that the same is true for 3-terminal off-state drain-source breakdown (BV_{ds}). This is primarily the result of two factors: decreased capacitive coupling between the SCFP and the GaAs due to the thicker dielectric between them and reduced bias (~6.5V) between the field plate and drain electrode in the source-coupled configuration.

Despite the ineffectual nature of the SCFP on breakdown voltage, it does provide significant benefit in terms of higher pulsed current; however, it does not begin to match that available with the GCFP. Both influence the surface depletion of the GaAs through trap occupancy [8], but only the GCFP dynamically modulates this surface depletion, thereby achieving higher pulsed current. Moreover, it does so even at microwave frequencies, despite the non-ideal character of the semiconductor surface passivation. The latter point is reinforced by the pronounced difference in RF transconductance for the two field plate configurations.

C_{gs} and C_{gd} illustrate further differences between field plate configurations. Both substantially increase C_{gs}, but they have the opposite effect on C_{gd}. In this manner the SCFP is clearly superior to the GCFP. The behavior is understood as follows. The GCFP increases C_{gs} due to the increase in electrical gate length and C_{gd} through the reduced separation between the gate and drain electrodes. The SCFP increases C_{gs} due to the parasitic MIM capacitance between it and the gate, while it decreases C_{gd} by shielding the gate electrode from the drain.

From the foregoing observations, there are several avenues available to improve performance of one or more parameters for the SCFP FET, but each of them involve unfavorable tradeoffs with other parameters. For instance, decreasing the SCFP dielectric thickness would improve breakdown, but not without unacceptably increasing C_{gs}. Alternatively, higher breakdown can be achieved with larger gate to

drain-side implant spacings, but pulsed current suffers, even when the dimension of the SCFP is increased equivalently. These and other factors in the fabrication process, including field plate dielectric composition and GaAs surface treatment, were varied in an effort to optimize the device performance. Yet none of them were successful in altering the tradeoffs beneficially.

Another approach is to combine a GCFP and SCFP. It offers the benefits of improved power performance of the GCFP with the reduced C_{gd} of the SCFP. At the same time, it has the immediately apparent drawback of increasing C_{gs} through the parasitic MIM capacitance between the field plates. Reducing the GCFP dimension or increasing the SCFP dielectric thickness can mitigate this. The results obtained by varying these factors are shown in Figure 4., demonstrating that both large- and small-signal RF performance can be simultaneously improved in this manner.

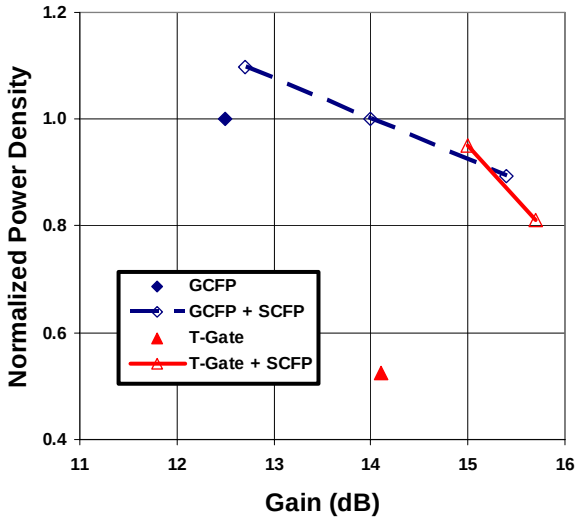

Figure 4. Saturated output power and gain comparison for FETs with different field plate configurations, dimensions, and dielectric thicknesses. All FETs have the same implant structure and gate length. Maximum saturated power requires both GCFP and SCFP.

Further improvement in microwave performance has been demonstrated through different tradeoffs in dimensional and processing factors. This work has shown that optimum performance can only be achieved with proper design of both gate-connected and source-connected field plate structures.

Conclusions

Source-connected and gate-connected field plates on planar GaAs HV MESFETs each offer distinctive benefits. Both provide improved microwave power density, but SCFPs do not match the degree of improvement available with GCFPs. Conversely, GCFPs degrade small-signal gain while SCFPs improve it. Best performance for both large- and small-signal operation is obtained simultaneously through a combination of both field plate configurations.

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Acronyms

ECP: Equivalent Circuit Parameter
GCFP: Gate-Connected Field Plate
MESFET: MEtal Semiconductor Field Effect Transisitor
MIM: Metal Insulator Metal
MIS: Metal Insulator Semiconductor
SCFP: Source-Connected Field Plate