Design and Fabrication of a Compact GaAs IPD Balun

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Abstract

Radio transceiver modules continue to shrink in size and cost, requiring novel approaches for integration of the numerous passive elements of the radio front-end. A center-tapped, 4:1 impedance transformed balun was designed and fabricated based on a GaAs Integrated Passive process for application to the 2.4 GHz ISM band. Die level glob topped results showed trade-offs in insertion loss and harmonic rejections based on changes of the input and output capacitance. Measured insertion loss of 0.91 dB, 2nd and 3rd harmonics of 12 dB and 23.7 dB, and common mode rejection ratio 25.7 dB were realized with the nominal design.

I. INTRODUCTION

Advanced modules for cellular phone applications continue to shrink in die size and cost, requiring novel approaches for integration of the numerous passive elements of the radio front-end [1]. Use of integrated passive devices on semiconductors offer the advantage of precise process control of the module elements as compared to ceramic based approaches, through fine line lithography and thin film deposition and etch processes, together with low cost associated with high volume batch processing. In this paper, the design and fabrication of an ISM band 4:1 balun based on a GaAs IPD process [2,3] is demonstrated.

II. BALUN DESIGN

Baluns have applications in signal conversion from balanced to unbalanced and vice versa. They are applied in transceiver modules or power amplifiers between the antenna and amplifier. Two types of baluns have been described extensively in the literature [5]; the Marchand-type using coupled transmission lines, and the conventional spiral transformers. For frequencies under 10 GHz, the size of the Marchand-type baluns are generally too large for RF module applications, thus spiral transformers are preferred. Our design uses spiral transformer and the design calls for low insertion loss, good balance, and appropriate size to fit specific real estate, at low cost.

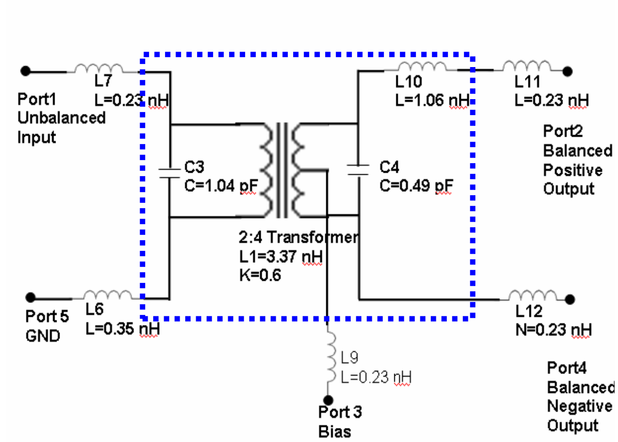

Figure 1. Schematic of 4:1 balun with wirebond inductors and matching elements.

The methodology for integrated passive design has been discussed in detail in references [1-3] and the need for a full-wave 3D electromagnetic simulation for assessing, and optimizing performance, as die size is reduced, has been emphasized. The balun schematic is shown in Figure 1, and the GaAs Integrated passive components fabricated are noted in the box of the schematic.

In order to meet the size specification of 1.1 mm by 0.9 mm, and impedance ratio 4:1, a balun with 2 turns in the primary and 4 turns in the secondary were chosen. An approximate design was first performed with the Agilent Design Systems (ADS) tool, using estimated lumped element values for the 2 x 4 turn balun. The balun design allowed a 50 ohms unbalanced input to transform to a balanced 200 ohms output. The primary and secondary inductances were estimated as 3.37 nH and 7.27 nH respectively, for a balun with internal diameter IDX and IDY of 200 um, with 10 um thick gold metal line, of width 25 um and space 10 um. Input capacitor C3 and output capacitor C4 were selected to tune the balun for low insertion loss in the 2.4 GHz band, and to ensure good input and output return losses. A center tap with near symmetric layout was provided at the output of the 2 x 4 balun for biasing the balun signals. Addition of this bias network required impedance adjustment at the output, so an inductor with inductance value 1.06 nH, was added. The size of the inductor was selected so overall transformer balun and additional components on the IPD die fitted the available space. Wirebond inductors, external to the IPD are L7, L11, L8, L9 and L12. These were used to further tune harmonic rejections of the balun. The S-parameters of the balun were generated by porting the whole layout of the IPD die into HFSS electromagnetic simulator. The simulator was previously calibrated with several measured inductors and capacitors to generate an IPD Library [1]. With the EM simulation, parasitic effects of interactions of close proximity components were all simulated.

III BALUN FABRICATION

The balun was fabricated on a 6-inch GaAs manufacturing line. Figure 2 shows a die photo of the fabricated balun on mechanical GaAs substrate. The process layer stack consists of metal 1 of 0.6 um evaporated gold; ILD1 a PECVD SiN dielectric for capacitors with MIM capacitor density 650 pF/mm2; MIM top plate or metal 2 of plated gold 2.5um; ILD2 of PECVD SiN 1000A; a metal 3 thick gold metal, 10um for inductor windings; and a final SiN passivation. The crossovers of inductor lines use air bridges over a stack of metal 1 and metal 2 underpasses.

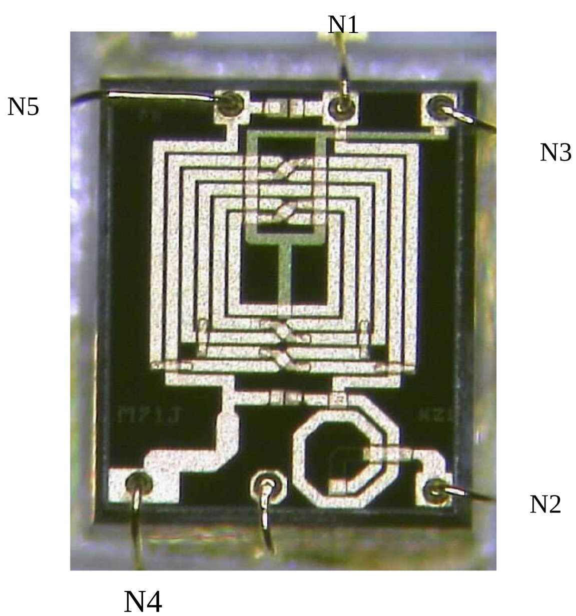

Figure 2. 4:1 ISM Balun die mounted for testing.

The completed wafers were thinned to 10 mils, sawn, die picked and assembled with conductive epoxy die attach to a metal flag and I mil gold wirebonds to calibrated 50 ohm probes. The probes are manufactured by JM Microprobe Company, Portland, Oregon, which also provides a calibration kit. Each probe assembly was grounded to the metal flag. Parametric measurements were taken from 500 MHz to 10 GHz on a 4-port RF Parametric Analyzer.

IV BALUN RESULTS AND ANALYSIS

The S4P measured parametric data was ported to ADS for final analysis to extract insertion loss and other balun parameters. In the die, N1 is the input unbalanced port, N3 is the bias port, N2 is the output balanced positive terminal, N4 is the output negative terminal, and N5 is grounded. Table 1 shows results of parameters extracted for a number of designs where the input and output capacitors were varied +/-5% and +/-10% from the nominal design to assess sensitivity. These designs are indicated M5, M10, NOM, P5, and P10 accordingly, in the table, and the results include the effect of protective glob over the die. The parameters consist of the insertion loss (IL); the second and third harmonics (H2) and (H3), the input and output return losses, common mode rejection (CMRR), amplitude and phase balance, and the effective phase imbalance. The balun insertion loss was determined with 50 ohm input termination at the unbalanced port, and 200-ohm termination at the output port transformed with an ideal 1:1 transformer at the output. The maximum differential insertion loss in the band increased or decreased as the capacitance values increased or decreased from the nominal value. The insertion loss S21, and the input, S11, and output, S22 return losses are compared to the HFSS simulation results in Figure 3 for the nominal design. The highest insertion loss is 0.91 dB at 2.48 GHz, and the minimum insertion loss at 2.4 GHz is 0.88 dB. The input and output return losses S11 and S22 were 14.9 dB and 17.2 dB, respectively. The 2nd and 3rd harmonic rejections were highest for the nominal design. The 2nd harmonic rejection was 12 dB for NOM and decreased to 8.86 dB for M5 and 9.7 dB for P10, while the 3rd harmonic rejection was 23.7 dB for NOM and decreased to 19.7 dB for M5 and 23 dB for P10. The simulation results are very close to the measurement results confirming accuracy of the models.

Table 1. Comparison of balun parameters for various variations of balun design. The capacitances C3 and C4 are varied +/- 5% and +/-10% from the nominal value for the designs in the table, where the nominal design is NOM, and the variations are M5, M10, P5 and P10. The balun parameters respond accordingly to the capacitance changes.

Design	**InsertionLoss (dB)**	**2nd Harm (dB)**	**3rd Harm (dB)**	**CMRR**	**Input Return Loss (dB)**	**Output Return Loss (dB)**	**Amplitude Balance (dB)**	**Phase Balance (Degree)**	**Phase Imbalance (Degree)**
M5	**-0.88**	**-8.86**	**-19.7**	**37.7**	**-13.3**	**-15.8**	**0.06**	**179.4**	**-0.60**
M10	**-0.86**	**-8.10**	**-18.6**	**37.3**	**-13.5**	**-15.9**	**0.08**	**179.2**	**-0.84**
NOM	**-0.91**	**-12.0**	**-23.7**	**25.7**	**-14.9**	**-17.2**	**0.18**	**183.3**	**3.30**
P5	**-0.98**	**-10.4**	**-21.9**	**34.2**	**-12.1**	**-13.6**	**0.08**	**180.6**	**0.60**
P10	**-1.03**	**-9.70**	**-23.0**	**32.1**	**-11.5**	**-12.6**	**0.21**	**180.4**	**0.40**

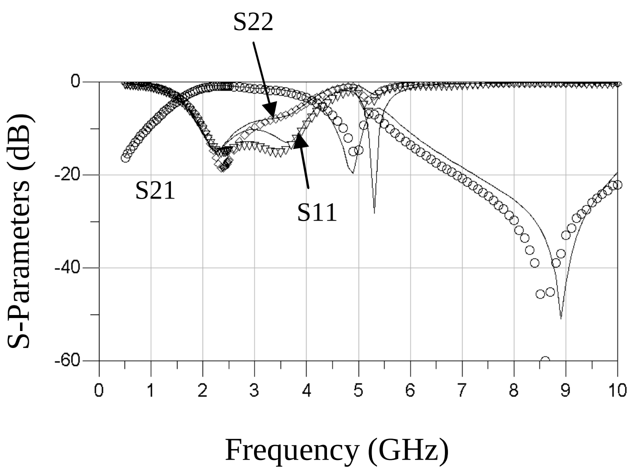

Figure 3. Comparison of measured (circle, triangle and square) and simulated (lines) insertion loss S21, and input, S22, and output, S11 return losses respectively, of ISM balun.

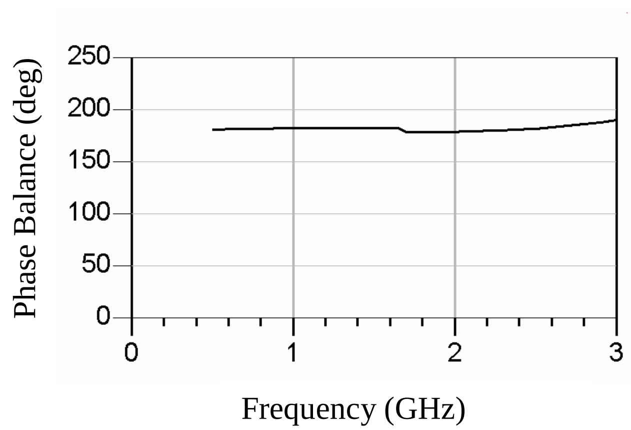

Figure 4 . Phase balance of balun over frequency range 500 MHz to 3 GHz..

The balun amplitude and phase balance were derived by terminating the output-plus terminal with 100 ohms and the output-minus terminal with 100 ohms, while the input unbalanced port was 50 ohms, and the bias port was grounded. The following equations were used.

Amplitude Balance = 20* log (S21/S31)

Phase Balance = Phase (S21) – Phase (S31)

Phase Imbalance = 180 – Phase Balance

The amplitude balance was 0.096 dB at 2.4 GHz and 0.176 dB at 2.48 GHz. The maximum phase imbalance within the band was 3.3 degrees. These numbers were within the design specifications.

Figure 4 shows the phase balance of the nominal design over frequency range 500 MHz to 3 GHz.

The common-mode rejection ratio is another important parameter also used to assess how well balanced the output terminal is with respect to positive and negative signals. For this determination, we used the approach where the output plus and minus terminals were connected to an ideal 1:1 transformer, terminated with 200 ohms. An ideal 180-degree phase shifter was inserted in series with the minus terminal before connection to the ideal transformer. This simulated feeding identical signals to the output balun ports. This is effectively equivalent to the derivation:

CMRR=20 * log ((S12-S13)/S12)

Common mode rejection ratio ranged from 25.7 to 37.7 dB with this design and variations meeting the criteria for the application. Figure 5 shows a trace of the common mode rejection ratio over 500 MHz to 5GHz. The higher the CMRR in the frequency band of interest, the well balanced the balun for the application.

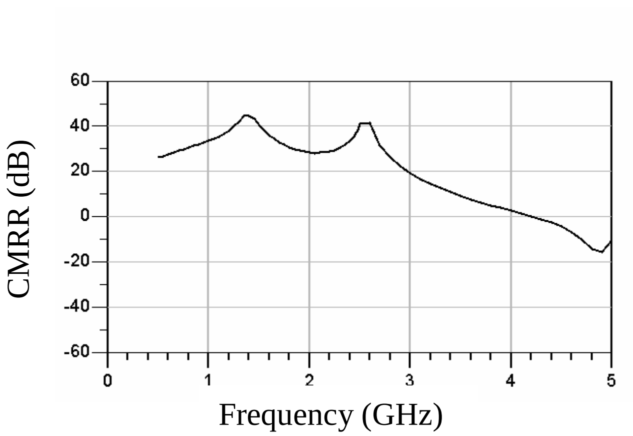

Figure 5. Common mode rejection ratio (dB) of ISM balun of nominal design over frequency 500 MHz and 5GHz.

V. CONCLUSION

Integrated passives based on semiconductor processes offer the advantage of excellent parameter control, and simplified and compact module component design A GaAs Integrated Passive Process (IPD) based on low cost mechanical grade GaAs LEC substrates was used to fabricate high performance balun transforming an unbalanced signal to balanced signal output in the 2.4 GHz ISM band, meeting design performance criteria. When compared to the ceramic based baluns, the present integrated passives for ISM band achieved in this paper are at least four times smaller in size, and measured results are closer to simulation.

VI ACKNOWLEDGMENTS

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ACRONYMS

IPD: Integrated Passive Devices
ISM: Industrial, Scientific and Medical
MIM: Metal Insulator Metal
ILD: Inter-level Dielectric
CMRR: Common Mode Rejection Ratio
LEC: Liquid Encapsulated Czochralski