InP DHBT technology for 100 Gbit/s applications

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Abstract

In this paper, we report a manufacturable InP DHBT technology, suitable for medium scale mixed-signal and monolithic microwave integrated circuits. The MBE grown InP-based DHBTs with an emitter area of $1 \times 4\ \mu m^2$ exhibited peak cutoff frequencies (f_T and f_{MAX}) > 300 GHz, and a breakdown voltage (BV_{CEo}) of ~ 5 V. The potential of this technology has been first assessed by the realization of a voltage controlled oscillator (VCO), exhibiting a high output power and a large tuning range. Subsequently, a demultiplexer (DEMUX) suitable for 100 Gbit/s fibre optical links, has been successfully fabricated and operated up to 110 Gbit/s.

INTRODUCTION

There has been a continuous interest in high-frequency devices for operation beyond 300 GHz. Prospective applications for these devices are high-speed analog, digital and mixed-signal integrated circuits (ICs) for signal processing and next generation communications systems. In particular, time-division-multiplexing (TDM) systems at data rates of 40 Gbit/s and beyond have been actively investigated to meet the increasing demands for high-speed and large transmission capacity.

Among various material and device candidates, a considerable work related to the design and fabrication of high-bandwidth, high-speed mixed signal ICs, has been carried out using III/V based high electron mobility transistors (HEMTs) [1] or heterojunction bipolar transistors (HBTs) [2,3]. Thanks to their material properties, InP-based DHBTs provide simultaneous high operation frequency, high breakdown voltage, good uniformity and reliability.

In this contribution, we report a manufacturable InP DHBT technology suitable for medium scale mixed-signal and monolithic microwave integrated circuits (MMICs). Using a previous generation technology (f_T ~ 250 GHz), we already have successfully demonstrated a set of analog and digital ICs operating up to 80 Gbit/s [4,5]. In the present work, the high-frequency InP-based DHBTs exhibit current gains in the range of 90 and cutoff frequency values of over 300 GHz. The potential of this technology has been confirmed by the fabrication and testing of a VCO and a DEMUX-IC suitable for ≥ 100 Gbit/s transmission systems.

TECHNOLOGY

The InP DHBT layer structures were grown on 3" semi-insulating InP substrates, in a multiwafer molecular beam epitaxy (MBE) system (GEN200). These structures feature an InP emitter, a graded InGaAs base, and a compositionally step-graded InGaAs/InGaAsP/InP collector, to minimize collector current blocking effects. Carbon and silicon were used for p- and n-type doping, respectively. The growth details have been reported elsewhere [6].

In contrast to most recent reports [7,8], based on aggressively scaled technologies (less than 0.5 µm), our fabrication process relies only on standard manufacturing techniques, including i-line stepper lithography and selective dry/wet etching. A detailed description of the device and IC manufacturing technology was reported in [9]. Briefly, the fabrication process is based on self-aligned base-emitter contacts and benzocyclobutene (BCB) for device passivation and planarization. The IC process is completed by NiCr resistors, MIM (metal-insulator-metal) capacitors, and three levels of Au-based interconnect metals. Figure 1 shows a top-view SEM (scanning electron microscopy) photograph of a nominal $1 \times 4\ \mu m^2$ DHBT.

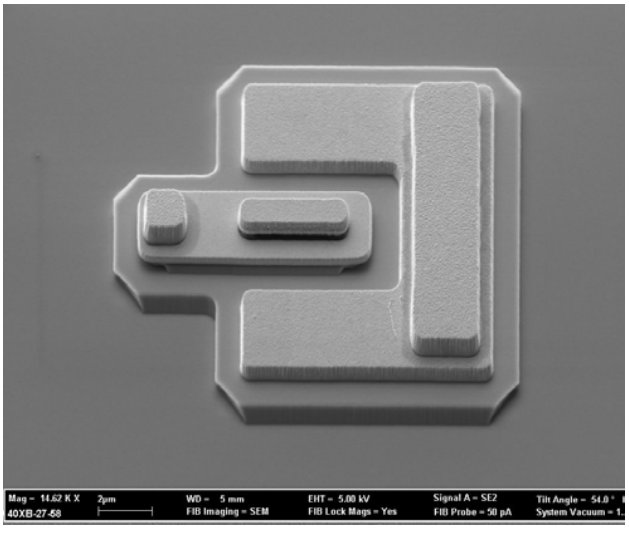

Figure 1: SEM-picture of an InP-DHBT before planarization. Emitter size: $1 \times 4\ \mu m^2$.

DEVICE PERFORMANCE

Figure 2 shows typical Gummel plots of $1 \times 4\ \mu m^2$ InGaAs/InP DHBTs. These devices displayed low leakage currents and current gains of $\beta \sim 90$. The InP DHBTs exhibited also breakdown voltages BV_{CEo} of about 5 V.

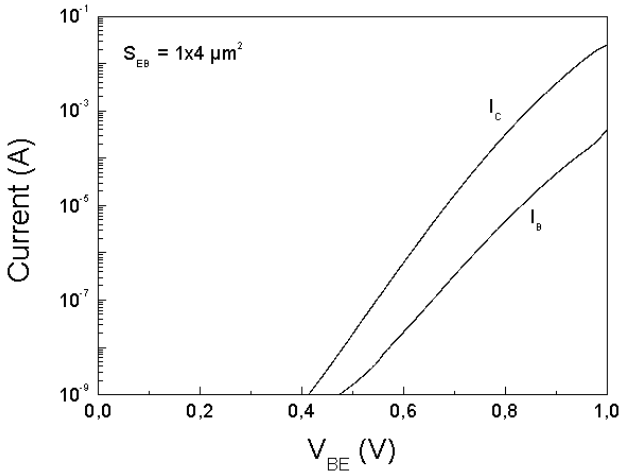

Figure 2: Typical Gummel-plots of InGaAs/InP DHBTs

The InGaAs/InP DHBTs have been manufactured with high yield (> 95%) and uniformity. Figure 3 illustrates the DC current gain distribution (β @ $V_{BE} = 0.9$ V) and its resulting variation across a 3" wafer, for 1 x 4 μm^2 emitter-size InGaAs/InP DHBTs, with mean values of 89 and a standard deviation of 7%.

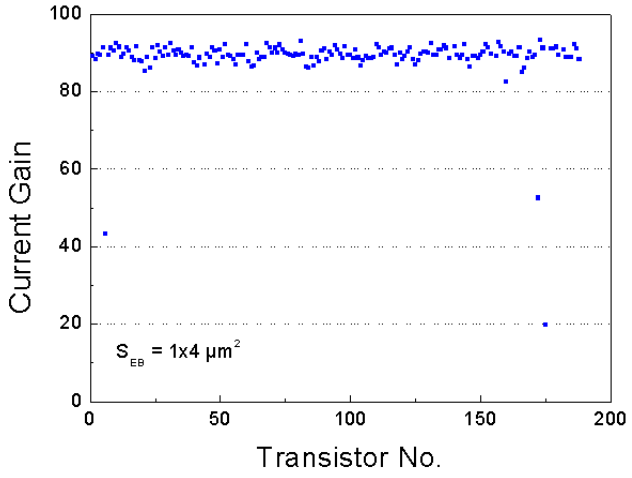

Figure 3: Current gain variation across a 3" wafer.

The microwave performance of these devices was characterized by on-wafer S-parameter measurements from 0.5 to 120 GHz. A typical frequency dependence of the current gain (h_{21}) and unilateral power gain (GU), of a $1 \times 4\ \mu m^2$ device, is shown in figure 4.

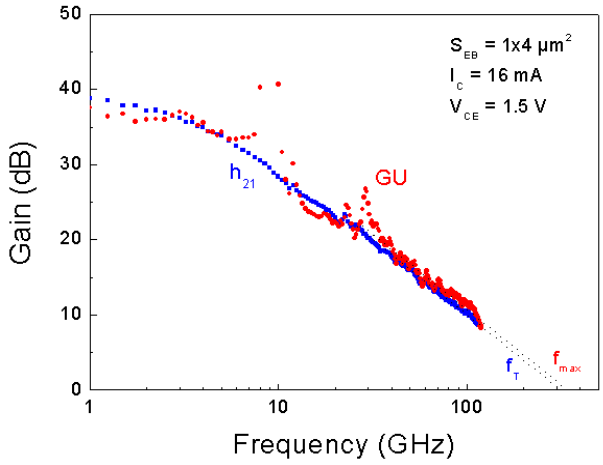

Figure 4: RF-properties of a $1 \times 4\ \mu m^2$ InGaAs/InP DHBT.

Using a –20 dB extrapolation, cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) values of over 300 GHz were measured at a collector current of 16 mA and a collector-emitter voltage of 1.5 V. The present device performance improvement, as compared to previously reported results in [9], is mainly attributed to the refinement of the layer structure and device layout.

CIRCUIT PERFORMANCE

Using this technology, a fundamental voltage controlled oscillator (VCO) suitable as a frequency source for ETDM (Electrical Time Division Multiplexing) with data rates beyond 40 Gbit/s, has been investigated. The VCO is a key building block for CDR (clock and data recovery) ICs, since it essentially contributes to the task of clock recovery. InP-based HBTs are well known for their good low-frequency noise [10] and have been recognized to be well suited for the millimeter-wave low-frequency noise oscillators [11].

The circuit architecture consists of a VCO core extended by an output buffer, whereas both circuit components are implemented in a differential topology. The circuit concept used for the VCO core is based on the so-called Colpitts-type architecture, thereby applying the negative resistance principle. In the resonator of the oscillator, short coplanar transmission lines represent inductively acting elements. Furthermore, transistor varactors are included in the resonator, thereby acting as the resonator capacitors as well as the voltage-controlled frequency tuning elements. More details regarding the functionality of the VCO circuit have been reported in [12].

The chip photograph of the realized VCO is illustrated in figure 5. The chip size is 1.25×1.25 mm², whereas most of the area results from the bias and high-frequency measurement pads. The total circuit has a complexity of only 9 active elements.

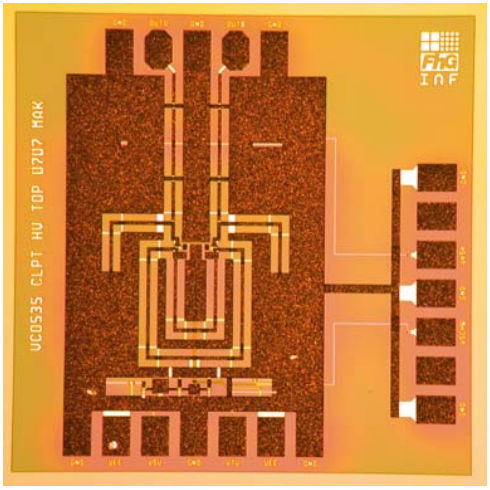

Figure 5: Chip photograph of an InGaAs/InP DHBT-based VCO. The chip-size is: 1.25 × 1.25 mm^2.

Figure 6 illustrates the tuning characteristic of the VCO with respect to the oscillation frequency (left axis) and the single-ended output power (right axis). According to this, the VCO can be continuously swept from 47 GHz to 58 GHz by varying the tuning voltage over 2.5 V, corresponding to a linear tuning bandwidth of 10 GHz. Within this tuning range, a single-ended output power up to +7 dBm is achieved, resulting in a differential signal power of +10 dBm. Referring to this achieved performance, the VCO is well suited for use in half-rate CDR circuits with data rates between 100 Gbit/s and 116 Gbit/s.

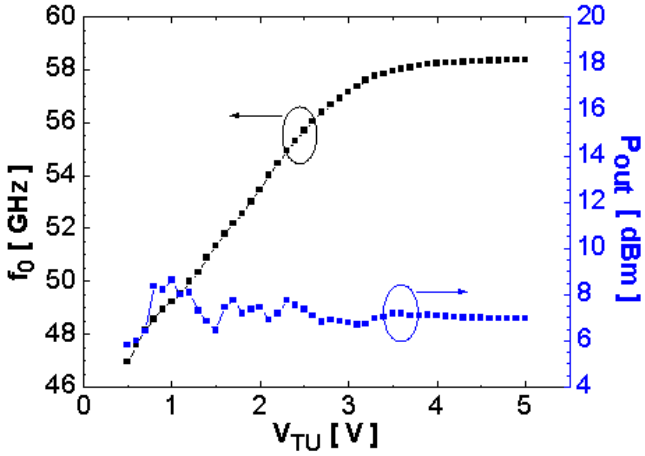

Figure 6: Oscillation frequency f_o and single-ended output power P_{out} vs. tuning voltage V_{TU}.

To evaluate this technology for more complex applications, a state-of-the-art 1:2 demultiplexer (DEMUX) has been designed and successfully manufactured. The core of the DEMUX consists of two parallel D-Flip-Flops (D-FF) in differential topology. Emitter coupled logic (ECL), as well as series-gating circuit techniques were used to achieve highest operation speed. The DEMUX core features a buffer (or amplifier) at its data and clock input, as well as, at its two data outputs. The input buffer is particularly critical for achieving a high sensitivity at the data input of the DEMUX. A chip photograph of the 1:2 DEMUX, comprising about 150 active components in a chip area of 1.75 × 1.5 mm^2 is shown in figure 5.

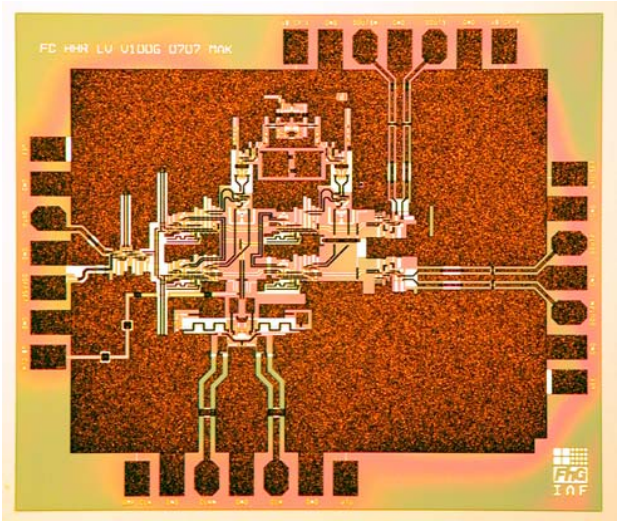

Figure 5: Chip photograph of the realized DEMUX circuit. The chip size is 1.75 × 1.5 mm^2.

Due to limited measurement capabilities, the IC has been tested only up to a data stream of 110 Gbit/s. Figure 6 illustrates the eye diagram of the 110 Gbit/s single-ended data signal used for driving the DEMUX. This input data signal features a voltage swing of 300 mV_{pp} at 110 Gbit/s, while the eye opening amounts to only about 84 mV_{pp}.

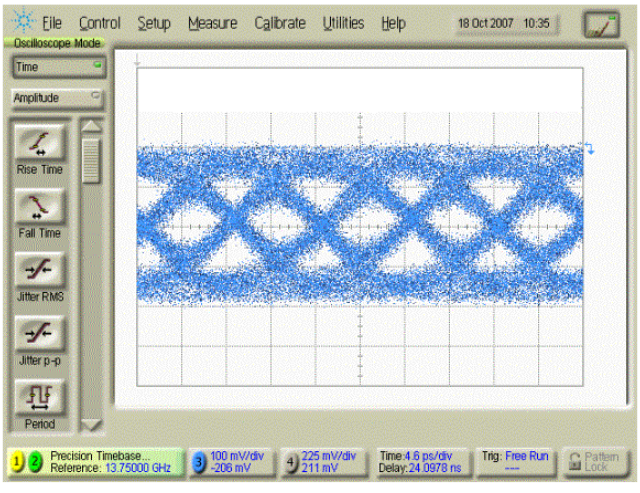

Figure 6: 110 Gbit/s single-ended data signal used for driving the DEMUX-IC.

Figure 7 illustrates the eye diagrams of the 55 Gbit/s single-ended data signals at the two output data channels of the DEMUX, with a voltage swing as high as 600 mV_{pp}. The clear eye opening indicates that higher bit-rates are to be expected. Nevertheless, these results confirm the great potential of InGaAs/InP DHBTs, and hold great promise for future optical communication systems, such as 100 Gbit/s Ethernet.

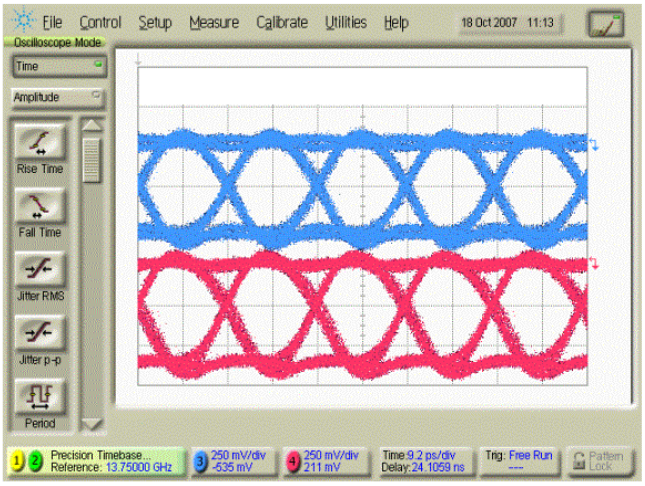

Figure 7: 55 Gbit/s demultiplexed data for a 110 Gbit/s input signal.

CONCLUSION

In summary, the development of a manufacturable InP DHBT technology, suitable for mixed-signal and monolithic microwave ICs, using standard fabrication procedures, has been reported. Devices with 1×4 μm^2 junction area exhibited current gains of 90 and cutoff frequencies over 300 GHz. A set of mixed-signal IC building blocks for ≥ 100 Gbit/s fibre optical links, including, VCOs and DEMUXs, have been successfully fabricated and tested. These results are promising for developing receiver modules for future optical transmission systems operating at 100 Gbit/s and beyond. In fact, the insight gained from the development of the 1:2 DEMUX as well as the VCO will be used for the design of a monolithically integrated CDR/DEMUX.

ACKNOWLEDGEMENT

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ACRONYMS

DHBT: Double Heterojunction Bipolar Transistor
MBE: Molecular beam Epitaxy
MMIC: Monolithic Microwave Integrated Circuits MIM:
MIM: Metal-Insulator-Metal
ECL: Emitter Coupled Logic
TDM: Time Division Multiplexing