Effect of Gate Edge Silicidation on Gate Leakage Current in AlGaN/GaN HEMTs

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Abstract

We have demonstrated a reduction in the gate leakage current of AlGaN/GaN HEMTs by suppressing gate edge silicidation. We found that the silicidation of Ni in the gate edge during formation of the SiN passivation film caused a lower work function and increased the gate leakage current. A NiOx barrier layer inserted between the gate electrode and passivation film prevented silicidation of the gate metal and drastically reduced the gate leakage current. We also determined that silicidation was prevented by a higher oxidation rate of NiOx. The gate leakage current was attributed to both the gate edge and Schottky junction. Moreover, we confirmed no initial degradation in a DC stress test at high temperature. These results indicate that suppressing NiSi formation has a key role in reducing the gate leakage current.

INTRODUCTION

AlGaN/GaN HEMTs have achieved good performance for high power applications, such as a power amplifier in wireless base stations. The requirement for high-power devices is primarily low gate leakage current for high-power operation and high reliability. We have previously reported that the absolute value of the gate leakage current is very important for the initial degradation of AlGaN/GaN HEMTs [1]. Further reduction in gate leakage current is required for next-generation networks.

In AlGaN/GaN HEMT structures, Ni and SiN are widely-used as materials for a Schottky gate electrode and passivation film, respectively. Thus, Ni and Si coexist around the edge of the gate electrode. We found that silicidation of the Ni gate edge can cause an increase in the gate leakage current because the work function of Ni is decreased by silicidation. Silicidation of the gate metal depends on the flow in which the gate metal and SiN passivation film are fabricated. When the gate metal is formed first and then SiN deposition by CVD follows later, more silicide can be formed during deposition. In the case of a T- or Y-shaped fine gate formed by electron-beam lithography for high-frequency devices, it may be preferable to form the gate metal before SiN deposition to prevent the gate length from expanding during dry or wet etching of the SiN passivation film [2-3].

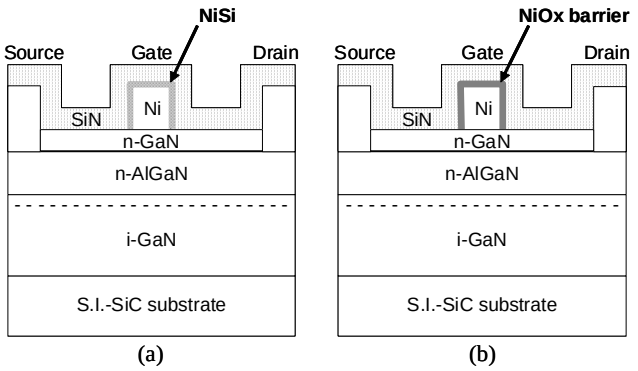

Fig. 1 Schematic cross-sectional view of (a) conventional and (b) our proposed AlGaN/GaN HEMTs.

In this paper, we have investigated the effect of gate edge silicidation on gate leakage current. We proposed the oxidized Ni barrier to suppress silicidation of gate edge. We have also investigated the control of the silicidation prevention through differences in the Ni oxidation method.

EXPERIMENTAL

Our developed AlGaN/GaN HEMTs consisted of an MOVPE-grown n-GaN/n-AlGaN/i-GaN structure, called a surface-charge-controlled structure, as shown in Fig. 1 [4]. By using an n-GaN cap layer, instead of an AlGaN layer, surface oxidation and frequency dispersion related surface instability could be prevented. Recessed ohmic technology was used to reduce the ohmic contact resistance [5]. An n-GaN cap layer was removed by RIE with Cl_2 gas before the evaporation of Ti/Al ohmic metal. Ohmic electrodes were annealed at a relatively low temperature of 550°C for 30 sec in N_2 ambient to keep the surface smooth. Photolithography

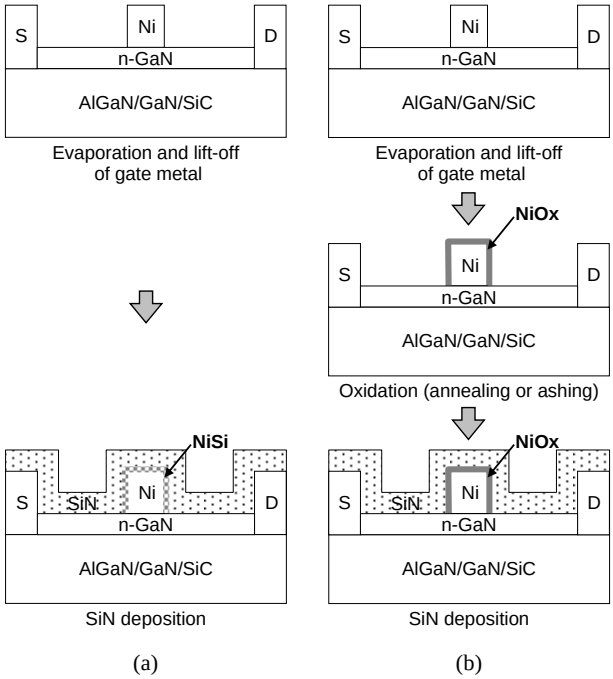

Fig. 2 Process flow diagrams of (a) conventional sample and (b) Ni-gate-oxidized sample.

TABLE I
EXPERIMENTAL CONDITIONS AROUND GATE EDGE

	Ni oxidation method
Sample *A*	Annealing
Sample *B*	O_2 plasma ashing
Sample *C* (Conventional)	None

was used to fabricate the gate electrode pattern using an i-line stepper. As the gate metal, a single layer of 100-nm-thick-Ni was formed by evaporation. The cross-sectional shape of the gate was a rectangle and the typical gate length was 1.2 μm. Electron-beam lithography was not used because of only confirmation of the effect of the gate edge.

After gate electrode fabrication, there are two main types of sample process for investigating the effects of suppressing gate metal silicidation. The process flow diagrams are shown in Fig. 2. In one procedure, SiN passivation film was deposited by PECVD just after gate electrode formation as a conventional flow. In the other process, we introduced Ni-gate-oxidized process just after the gate electrode was fabridated. After oxidation, SiN was deposited.

In this paper, we have fabricated three kinds of samples, as listed in Table I. Samples *A* and *B* had the aforementioned NiOx barrier layer, while sample *C* used as a reference, did not. In addition, two Ni oxidation methods were investigated. Sample *A* was annealed in the atmosphere at 350°C and sample *B* was oxidized by O_2 plasma ashing with power of 300 W.

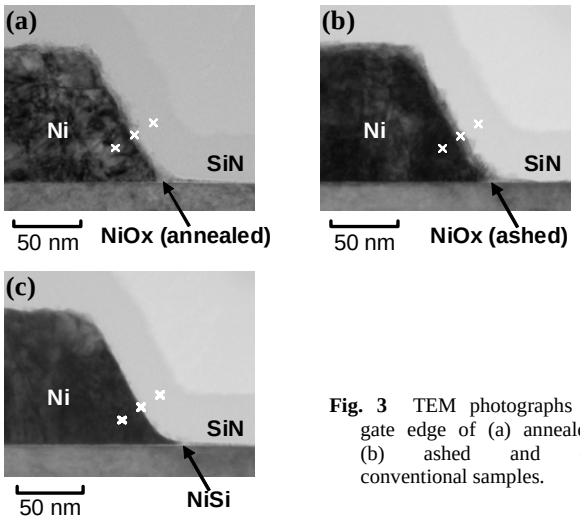

Fig. 3 TEM photographs of gate edge of (a) annealed, (b) ashed and (c) conventional samples.

RESULTS AND DISCUSSIONS

Cross-sectional TEM photographs of the gate edge and EDX results are shown in Figs. 3 and 4, respectively. The EDX measurement points are indicated in Fig. 3. Three points on the Ni side, interface, and SiN side were measured in each TEM photograph. The EDX analysis results were compiled for four elements: Si, O, Ni, and N. According to the TEM photographs, there were other layers at the interface between the Ni gate and SiN passivation film in all the samples. The TEM photographs also indicate that the thickness of intermediate layer at the interface in samples *A* and *B* were almost the same.

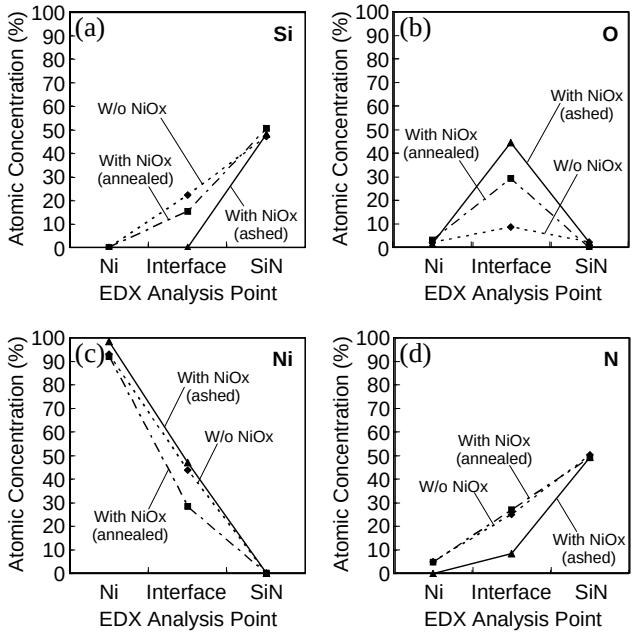

Fig. 4 Atomic concentration measured by EDX. Results are compiled for each element: (a)Si, (b)O, (c)Ni and (d)N.

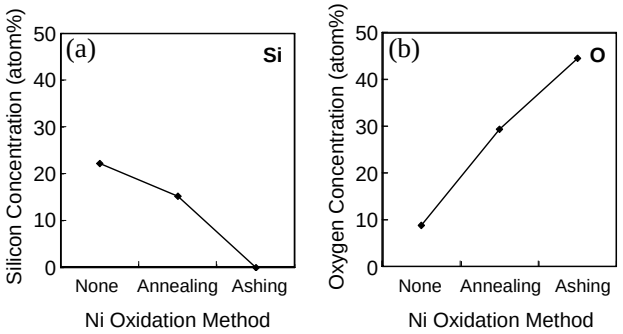

Fig. 5 (a) Silicidation ratio and (b) oxidation ratio of a gate edge in AlGaN/GaN HEMT measured by EDX.

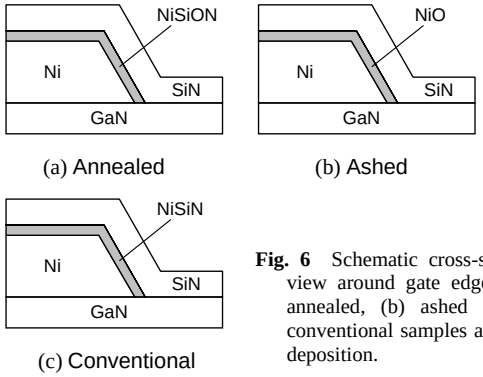

Fig. 6 Schematic cross-sectional view around gate edge of (a) annealed, (b) ashed and (c) conventional samples after SiN deposition.

When we focused attention on interfacial oxygen, we found that the conventional sample (*C*) has hardly been oxidized, as shown in Fig. 4(b). On the other hand, annealed and ashed samples (*A* and *B*) had clearly been oxidized. However, the ashed sample had a higher oxidation ratio than the annealed sample. Next, in the case of silicon and nitrogen, both Si and N diffused to the interfacial layers in the conventional and the annealed samples, and NiSiN and NiSiON were formed in them, respectively. However, the content rate of Si and N at the interfacial layer in the ashed sample was very low, and distinct NiOx was formed. The silicidation and oxidation ratios produced by differences in the Ni oxidation process are shown in Fig. 5. The silicidation ratio increased and the oxidation ratio decreased in the sample order: conventional, annealed, and ashed. Figure 6 shows the summary of the composition of intermediate layer in three samples.

The two-terminal gate leakage currents under forward and reverse bias are shown in Fig. 7. The gate leakage current was remarkably different between samples with and without the NiOx barrier under both forward and reverse bias. The conventional sample had a lower Schottky barrier than the Ni oxidized samples, as shown in Fig. 7(a). It was understood that the low Schottky barrier height of the gate edge silicide was dominant and reduced total barrier height drastically even if the silicide was formed only at the gate edge. This lower barrier height of the conventional sample also caused a larger gate leakage current under reverse bias. The NiOx barrier layer for preventing gate edge silicidation has a profound effect on gate leakage current reduction. Next, a different Ni oxidation method was compared. In the annealed and ashed samples, the gate leakage currents under forward gate bias were almost the same. However, under reverse gate bias, the gate leakage current of the ashed sample was lower than that of the annealed one above 10 V. It seems that this was caused by the quality of the foregoing NiOx barrier. The silicidation ratio of the annealed sample was larger than that of the ashed sample at the Ni-SiN interface, so the interfacial silicided layer can be a leakage pass under a higher gate bias. The annealing-induced oxidation in this study was insufficient to suppress the gate silicidation and the gate leakage current. We found that high oxidation ratio in NiOx barrier is very important for suppressing the gate silicidation and gate leakage current.

Figure 8 show the I_d-V_{gs} and g_m-V_{gs} characteristics. The threshold voltage of the sample with the Ni oxidation process was shallower than that of the conventional sample because of the lower Schottky barrier height. The gate edge silicidation also affected the threshold voltage. As shown in Fig. 8(a), the I_d of the ashed sample was lower than that of the annealed sample under forward gate bias because of the lower g_m. This may be caused by the tapered shape of the gate edge, as shown in Fig. 3 and 9. Because a relatively large area of the tapered gate edge was oxidized, electrons could have been trapped in the NiOx under the forward gate bias. Higher oxidation ratio of ashed sample than annealed

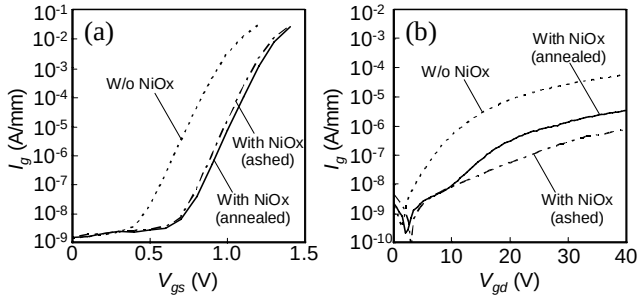

Fig. 7 (a) Forward and (b) reverse gate leakage characteristics of annealed, ashed and conventional AlGaN/GaN HEMTs.

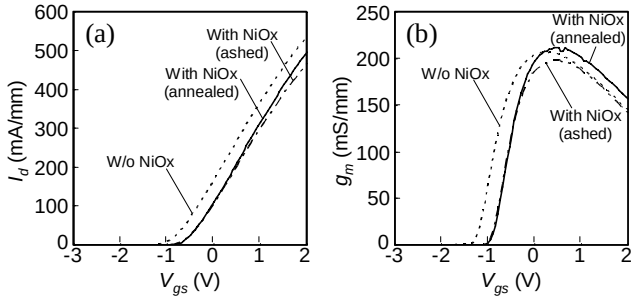

Fig. 8 (a) I_d-V_{gs} and (b) g_m-V_{gs} characteristics of annealed, ashed and conventional AlGaN/GaN HEMTs.

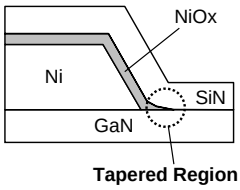

Fig. 9 Schematic cross-sectional view of tapered gate shape in AlGaN/GaN HEMTs.

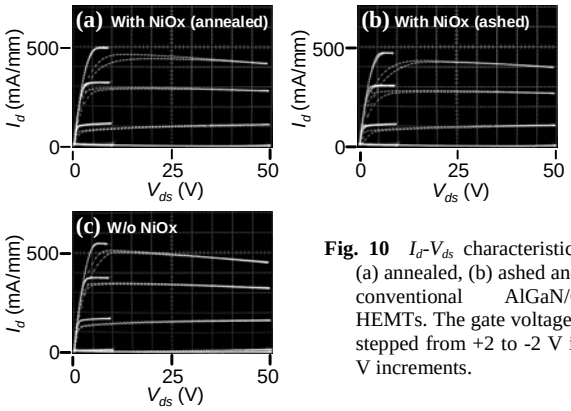

Fig. 10 I_d-V_{ds} characteristics of (a) annealed, (b) ashed and (c) conventional AlGaN/GaN HEMTs. The gate voltage was stepped from +2 to -2 V in -1 V increments.

one might be attributed to more trapped electrons.

The three-terminal I_d-V_{ds} characteristics are shown in Fig. 10. The I_d decreased and the current collapse increased in the sample order: conventional, annealed, and ashed. These phenomena might be also originated from oxidation of the gate edge with a tapered shape. To prevent the decrease in drain current and the increase in current collapse, a vertically shaped gate edge is necessary. For example, a tri-level resist is effective.

The study of initial degradation phenomenon is important for commercialization. An on-wafer pinched-off DC stress test under the high temperature of 150°C was investigated, as shown in Fig. 11. For the process around the gate edge, the sample with NiOx barrier was oxidized by annealing in the atmosphere. No sudden degradation was observed for up to 2000 sec. in both samples. However, the gate leakage current of the sample without NiOx barrier was unstable and gradually changed. This result indicates that the NiOx barrier might achieve both small gate leakage current and high reliability.

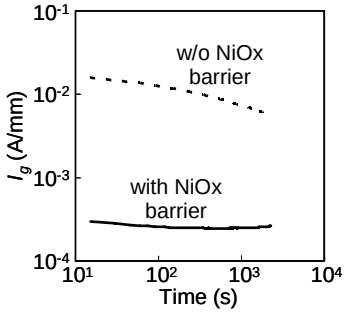

Fig. 11 On-wafer DC stress test at 150°C. V_{ds} and V_{gs} were 50 V and -5V, respectively. I_g was monitored during this test.

CONCLUSIONS

We have found that the silicidation of the gate edge occurs in AlGaN/GaN HEMTs and causes an increase in the gate leakage current. We have proposed the NiOx fabricated by gate metal oxidation as a barrier layer between Ni and SiN and demonstrated a reduction in gate leakage current. The content ratio of oxygen in NiOx is important for suppressing the silicidation. In our oxidation conditions, ashing was able to prevent silicidation and reduce the gate leakage current better than annealing. In a pinched-off DC stress test, no initial sudden degradation was observed. We conclude that controlling the gate edge silicidation is very important for gate leakage current reduction in the AlGaN/GaN HEMT structure.

ACKNOWLEDGEMENTS

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ACRONYMS

HEMT: High Electron Mobility Transistor
CVD: Chemical Vapor Deposition
MOVPE: Metal-Organic Vapor Phase Epitaxy
RIE: Reactive Ion Etching
PECVD: Plasma Enhanced Chemical Vapor Deposition
TEM: Transmission Electron Microscope
EDX: Energy-Dispersive X-ray Spectrometer