Technology for Non-Recessed Short Gate Length E-Mode AlGaN/GaN High-Electron Mobility Transistors

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INTRODUCTION

In the fabrication of AlGaN/GaN HEMTs, silicon nitride (SiN_x) is often used for a variety of purposes, such as passivation layer and field-plate dielectric layer to name a few [1,2]. Nitride deposition, as a processing step, is usually done before gate fabrication. Subsequent gate fabrication is carried out by removal of the nitride from the gate footprint area [3]. The nitride removal, being a highly anisotropic process, is effectively performed using fluorine-based plasma etching in RIE plasma systems. In order to ensure complete removal of nitride, significant over etching is done. During this over etching period the epilayer is subject to fluorine plasma bombardment, which has been found to have multiple advantageous effects on the performance of AlGaN/GaN transistors. Foremost is the positive shift of threshold voltage as a consequence of CF_4 bombardment. SIMS has shown an abundance of fluorine atoms in the epilayer. The incident fluorine ions, speculated as negatively charged, can effectively raise the AlGaN barrier potential and hence can deplete the channel charge thereby moving the threshold voltage to positive values. It has already been demonstrated that for 1 μm gate length devices, positive threshold voltage is obtainable, leading to E-mode operation of devices [4]. This is a significant achievement as in this procedure E-mode devices can be obtained without recessing the gate region, which is a difficult processing step in terms of controllability. Another prior work has shown that a combination of recessing technology and fluorine plasma treatment can result in high performance E-mode devices [5].

E-mode devices are normally off thereby eliminating the necessity of negative standby voltage supply. This will lead to substantial decrease in standby power and reduction in circuit complexity. Furthermore, monolithic fabrication of D-mode and E-mode devices for realization of digital circuits can also be implemented without complicated processing steps.

Transistor speed is most directly dependent on its gate length. In order to realize high performance digital circuits both E-mode and D-mode devices having short gate length (sub-micron and shorter) is desirable. This work demonstrates for the first time the methodology of obtaining short gate length E-mode devices solely by fluorine plasma treatment (i. e. without any gate recessing).

EXPERIMENT

The structure used in this letter was grown on semi-insulating 6H-SiC substrates by metal–organic chemical vapor deposition. It consisted of an AlN nucleation layer, 2.0 μm undoped GaN, and a 20 nm $Al_{0.3}Ga_{0.7}N$ barrier layer. Hall measurements showed sheet carrier concentration of 1.1×10^{13} cm^{-2} and an electron mobility of 1300 cm^2/V-s at room temperature on as-grown wafers. The first step for device fabrication was mesa-isolation using Cl_2/Ar plasma in an inductively-coupled-plasma reactive ion etch system. Ti/Al/Mo/Au ohmic metallization with a total thickness of 160 nm was evaporated and annealed. In this particular experiment the entire region between source and drain was treated in CF_4 plasma under different DC self-bias in an RIE system. Gate-footprints 0.25 μm and sidelobes were then patterned using trilayer PMMA and e-beam lithography, followed by Ni/Au (300/2500 Å) gate-metal evaporation. Finally, an overlay metallization was deposited for probing pads. The devices had a gate width of 100 μm. An annealing

step was done in RTP at 500 °C for different duration to shift the threshold voltage.

RESUTLS AND DISCUSSION

Obtaining E-mode devices with short gate length and without recessing is particularly difficult because with the shortening of gate length, the modulation efficiency of the gate decreases. Therefore, it becomes increasingly difficult for the

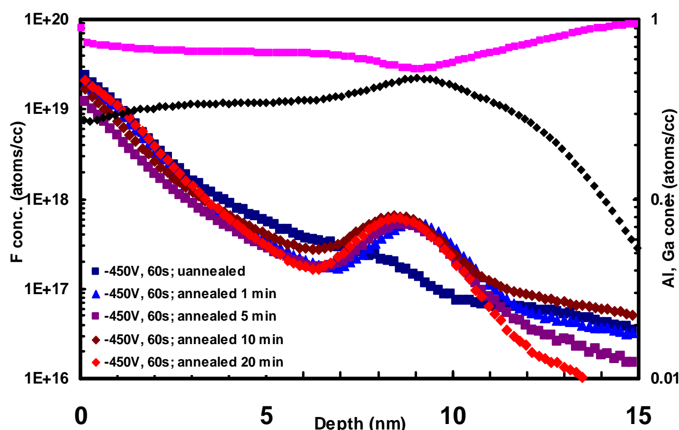

Fig. 1 Secondary Ion Mass Spectrometry data showing the presence of fluorine inside the heterostructure after plasma bombardment. The fluorine peak at the channel is very stable; it does not move even after lengthy annealing.

gate potential to modulate the channel potential. In the presence of implanted fluorine ions due to plasma treatment (Fig. 1), the modulation capability of the gate is further jeopardized as the

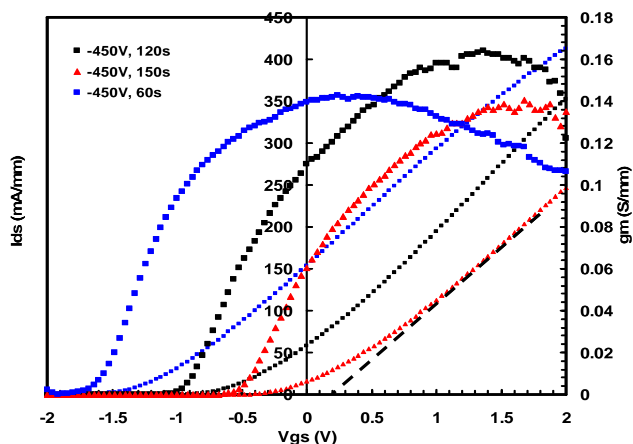

Fig. 2 Shift of threshold voltage for different bombardment duration (shown in the legend). 150s bombardment causes the largest shift in threshold voltage. All results are after annealing at 500 °C in a rapid thermal annealing system.

immobile fluorine ions bend the energy band in the barrier layer. A very fine tuning of fluorine induced potential is required in order to restore effective gate modulation of the channel leading to E-mode device operation. The presence of fluorine in the barrier layer affects the mobility and sheet concentration values. In order to ensure high transconductance and low on-resistance device characteristics, optimum values of mobility and sheet concentration have to be obtained in the 2DEG channel. Therefore, understanding the mobility and sheet concentration behavior as a result of different bombardment bias is crucial to designing high performance E-mode devices.

Table 1

Group (yr.)	L_g (mm)	$I_{d,max}$ (mA/mm)	g_m (mS/mm)	V_{th} (mV)	Approach
HRL (02)	0.2	100	85	0	Recessed
UIUC (03)	1	470	248	75	Recessed
Fujitsu (04)	0.12	380	230	0	Non-recessed
UIUC (05)	1	505/ 455	345/ 310	350/ 470	Recessed / After gate annealing
HKUST (05)	1	310	148	900	CF_4 treatment
UCSB (06)	0.16	1200	400	100	CF_4 treatment + Recess
This work	0.25	250	140	220	CF_4 treatment

Table 1 Comparison of devices fabricated in this work with previous works.

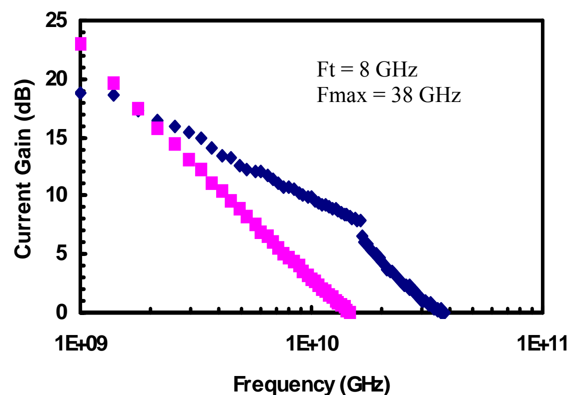

Fig. 3 Short-circuit current gain (|$h21$|) and unilateral power gain of a 0.25 μm × 100 μm E-mode AlGaN/GaN HEMT.

Our results indicate that fluorine treatment followed by annealing can effectively shift the threshold voltage up to 4 V (from about -3.8 V without any plasma treatment to 0.22 V) in a 0.25 µm device (Fig. 2). We observed that the threshold voltage shift was dependent on fluorine bombardment dose and annealing time. A comparison of DC characteristics ($I_{d,max}$, g_m, V_{th}) to reported results from other groups has been shown in Table 1. Although our first generation devices demonstrated modest performance of 148 mS/mm of transconductance and I_{dmax} of 250 mA/mm with a V_{th} of 0.22 V, this is the first 0.25 µm AlGaN/GaN E-mode HEMT obtained by fluorine plasma treatment only. One of the reasons that maximum current and transconductance are low is because of the plasma bombardment in the entire region between source and drain. Plasma based incorporation of fluorine in these regions decrease sheet concentration and hence, increases the sheet resistance. Ideally, only the gate foot-print area needs to be treated with plasma as reported in [4]. Due to the same reason a very low value of Ft (8GHz) and Fmax (38 GHz) were obtained (Fig. 3).

CONCLUSION

Preliminary results show that E-mode devices can be obtained in short gate length AlGaN/GaN HEMTs using plasma treatment and without gate recessing. The positive threshold voltage shift is dependent on plasma self-bias voltage, annealing time. Dependence on annealing temperature is also expected and further investigations are needed. Further improvement in HEMT performance is possible by further process improvements together with plasma treatment only in the gate region.

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ACRONYMS

HEMT: High Electron Mobility Transistor
E-mode: Enhance Mode
D-mode: Depletion Mode
RIE: Reactive Ion Etching
SIMS: Secondary Ion Mass Spectrometry