A Surface Treatment Technique for III-N Device Fabrication

Yun Zhang, Jae-Hyun Ryou, Russell D. Dupuis, and Shyh-Chiang Shen

School of Electrical and Computer Engineering 777
Atlantic Drive NW, Atlanta, GA 30332-0250 Phone:
404-894-1884; Email: shensc@ece.gatech.edu

Keywords: III-N, SURFACE TREATMENT, ELECTRODE-LESS WET ETCHING, DOE

Abstract

In this paper, we present a simple yet effective surface treatment technique using a UV-enhanced electrode-less wet-etching to reduce roughness as well as surface leakage paths in ICP-etched III-N devices. The surface treatment in this study utilizes an aqueous solution with potassium hydroxide (KOH) as the etchant, catalyzed with a UV-light illumination. To study optimal conditions of the surface treatment, bi-level design of experiments were studied and an optimal etching conduction was found to achieve a reduction of the leakage current in III-N p-n junctions by at least one order of magnitude.

INTRODUCTION

Preparing a high-quality III-N surface, either before the epitaxial growth or during the fabrication processing, plays an important role in achieving high-performance III-N devices. Mesa etching is the main processing step that will reduce the quality of material surface. Plasma-based dry etching methods such as ICP and RIE often induce ion damage to the device surface as well as mesa sidewalls. Consequently, these methods may decrease the device performance with an increase in surface leakage. Wet etching techniques, on the other hand, is an alternative to dry etching in order to reduce plasma-induced surface damage; however, conventional chemical wet etching, such as BOE or HCl, does not work to high-quality III-N material. Some groups have reported studies on photoelectrochemical (PEC) etching [1-6] and/or ultraviolet-assisted wet etching [7-9] as replacements to plasma etching.

Wet etching in III-N materials still leaves two problems. First, UV-assisted wet etching is a selective etching to *n*-type III-N material. The etching rate on *p*-type III-N material is not obvious so it cannot be use to fabricate mesa on *p*-type material. Secondly, typical UV-assisted wet etching tends to have higher etching rate on the sites where the defect density is high. The wet-etching techniques are typically used for the defect density study on n-type III-N materials rather than achieving high-uniformity etching surface in fabrication processing. Recently, Balarge's group demonstrated a possibility of using a diluted KOH/$K_2S_2O_8$ solution to achieve binary etching on intrinsic, p-type, and n-type GaN layers [10]. The low etching rate with such solutions not only provides tight control of the III-N HFET but also reveals the possibility to use it as a useful surface treatment technique. The efficacy of using this new wet-etching chemical system for the surface treatment on III-N minority-carrier devices, however, is yet studied.

To develop a suitable fabrication processing for III-N PN junction, in this study, we used an ICP dry etching for p- and n-layer mesa etching. The n-type surface is then treated in a UV-assisted wet etching treatment to remove only a few mono-layers of III-N surface atoms and to improve leakage current characteristics. In contrast to conventional PEC etching, we used the potassium persulphate ($K_2S_2O_8$) as the oxidant to lift the need for electrodes in the UV-assisted surface treatment step. To achieve a smooth surface morphology with reduced high-filed leakage current, a set of design of experiments was conducted by studying the correlation between UV illumination power, KOH concentration, and the $K_2S_2O_8$ concentration. The results showed that, through this new surface treatment technique, we were able to achieve an improvement of surface morphology by > 75% and at least 10-times lower leakage current on GaN PIN diodes. The electrode-less UV-enhanced surface technique may provide a simple yet effective way to fabricate low-leakage III-N devices.

EXPERIMENT

A three-factor two-level DOE study on *n*-type GaN wet etching was conducted to determine an optimal etching recipe. Before wet etching, eight GaN samples cut from a 2inch sapphire wafer were mesa etched by BCl_3/Cl_2 in an ICP system. The etching depth was 1000 À with an etching rateof 1000 À/min. These etched samples were used to study an optimal surface treatment with the electrode-less UV-assisted wet-etching technique. KOH concentration, $K_2S_2O_8$ concentration, and UV light power were three experimental variables for the surface treatment study, and were designed to a two-level variation: high level (H) and low level (L), respectively. This gave a total of eight different etching conditions in this DOE study. Each sample was randomly assigned to one of the eight etching conditions. All the chemicals were freshly prepared in DI water just before each wet etching, and the chemical reaction went at room temperature.

The etching time was set to 5 min for each etching condition. Due to the variation in the surface smoothness due to the ICP etching, we used the percentage of surface roughness improvement before and after the surface treatment as the output response. Surface roughness (RMS in nm) is measured by AFM before and after ICP etching. The positions of the AFM scan were recorded so that the same location could be analyzed for valid comparison. Each sample was surface-treated using one of the 8 etching conditions and a post-wet etching AFM scan was evaluated to determine the surface treatment effectiveness. The surface morphology improvement is defined as: RMS improvement (□RMS in %) = [(RMS before wet etching) - (RMS after wet etching)] / (RMS before wet etching). The DOE designs and the responses on the changes in surface roughness are summarized in Table I.

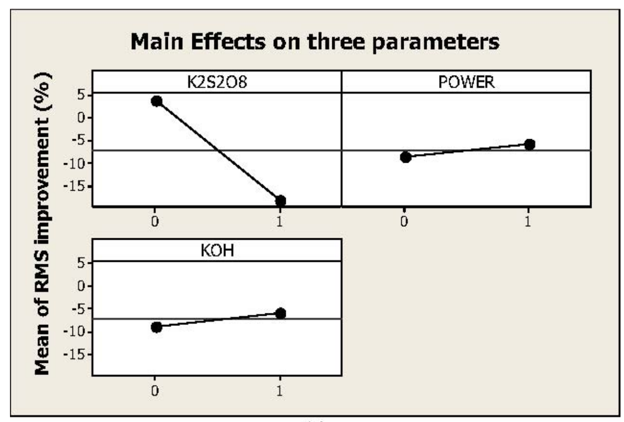
TABLE I THE DESIGN OF EXPERIMENTS OF THE VARIABLES USED IN THE SURFACE TREATMENT STUDY AND THE SUMMARY OF THE RESPONSE

#	UV	KOH	$K_2S_2O_8$	RMS (nm) before wet etching	RMS (nm) after etching	□RMS (%)
1	H	L	L	0.390	0.378	3.07
2	H	H	L	0.385	0.348	9.61
3	H	L	H	0.315	0.340	-7.93
4	H	H	H	0.272	0.349	-28.3
5	L	L	L	0.281	0.344	-22.41

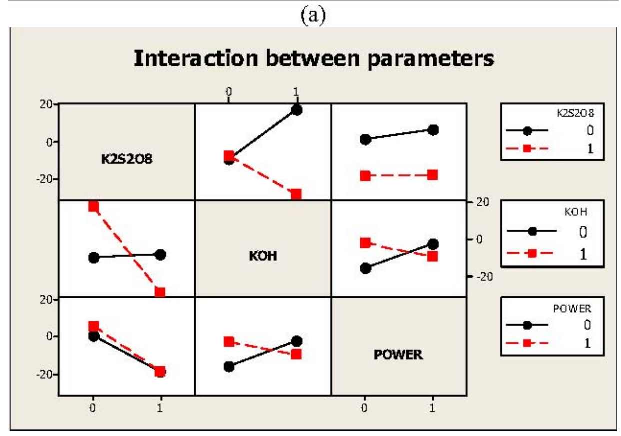
RESULTS AND DISCUSSIONS

In Table I, we observed that some etching conditions results in worse surface roughness, which corresponds to a negative value in the □RMS, possibly due to aggressive etching and/or the presence of dislocation defects. With proper choices of etching conditions, however, smooth surface may be achieved. To study the correlation between controlling variables, the main effect and their interactions were plotted in Figure 1 (a) and Figure 1 (b).

Figure 1 (a) is a set of plots showing the main effects of KOH concentration, $K_2S_2O_8$ concentration, and the UV illumination power on the surface roughness improvement in the bi-level DOE. The data points were averaged for each level for parameters specified on top of each graph. The "L" level corresponds to "0" and the "H" level corresponds to a "1" in each plot. It is observed that the $K_2S_2O_8$ concentration has a significant effect: lowering the $K_2S_2O_8$ concentration can improve the surface uniformity. Figure 1 (b) is a set of plots showing the interactions between [KOH], [$K_2S_2O_8$], and the UV illumination power in the DOE. Variables in the diagonal boxes indicate the parameters used in the x-axis of each column. The interactions with the variable indicated in the row are shown with solid circles for the "H" levels and solid squares for the "L" levels, respectively. We can see that $K_2S_2O_8$ and KOH have significant interaction. KOH concentration is also significant but its effect varies with different $K_2S_2O_8$ concentration level. In etching conditions with low $K_2S_2O_8$ concentration, higher KOH concentration may yield smoother surface. On the other hand, if $K_2S_2O_8$ concentration is high, the higher KOH concentration produces a rougher surface. We found that an effective wetetching-based surface treatment may be achieved with a $K_2S_2O_8$ concentration in the vicinity of "L" level and a KOH concentration around the "H" level. The UV illumination power however may not be a dominate factor.



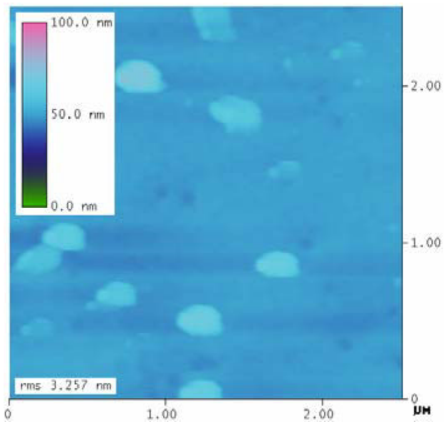
(a)



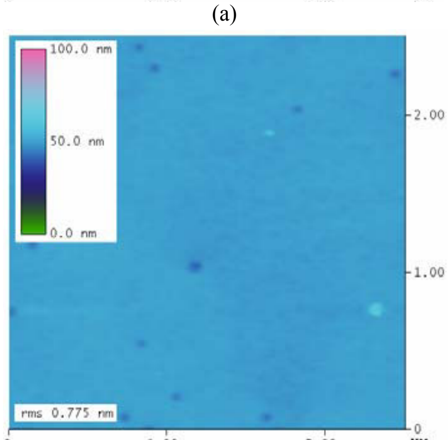
(b) Figure 1. (a) Main effects of KOH, $K_2S_2O_8$, and power to surface roughness improvement (b) Interaction effects between KOH, $K_2S_2O_8$, and power to surface roughness improvement.

Using an optimal etching condition for surface treatment determined in this DOE, Figure 2 (a) and (b) showed the AFM pictures of n-type GaN etched surface taken before and after the surface treatment, respectively. We found that the surface roughness is improved by ~75% after the surface treatment when compared to the non-treated, ICP-etched surface (with RMS value reduction from 3.527 nm to 0.775

nm). In Figure 2 (a), there are some "spikes" induced by dry etching but they were effectively removed by the surface treatment, as shown in in Figure 2 (b). This clearly shows the ability of the proposed surface treatment technique for effective surface morphology modification



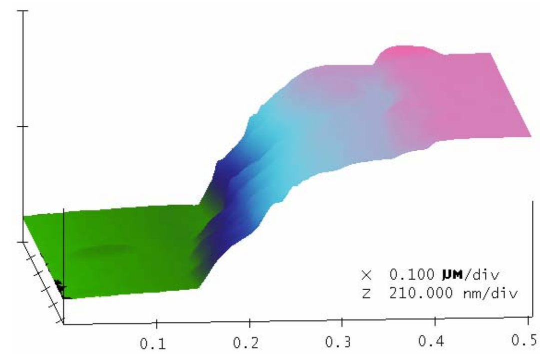
(a)



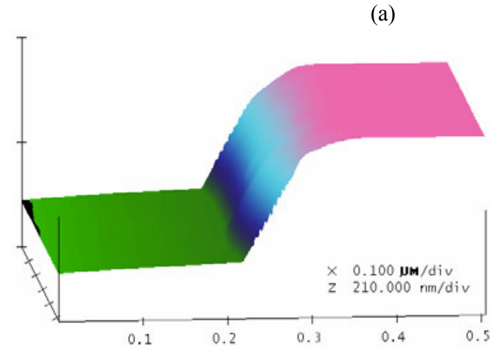
(b)

Figure 2. 2D AFM plots showing the ICP-etched n-type GaN surface (a) before the surface treatment and (b) after the surface treatment

Figure 3 shows 3D AFM images of etched mesa sidewall morphology before and after wet etching. It is clear to see that the wet etching reduced the tapered mesa sidewall width from 200 nm to < 100 nm. In addition, a much smoother sidewall was obtained as well. To study the efficacy of the side-wall leakage suppression, we fabricated GaN PIN diodes grown on SiC substrates with two of the surface treatment conditions. The results were compared with those devices fabricated without the surface treatment. Typical reverse-biased I-V curves with various etching conditions are shown in Figure 4 (under the dark condition). We found that, with a proper choice of surface treatment condition, the leakage current in PIN diodes can be reduced by at least one order of magnitude. The device breakdown voltage was extended to a higher voltage and catastrophic breakdown was not observed with surface-treated samples. Using this surface treatment technique, we have applied this processing module in standard device fabrication processing and fabricated III-N HFET and GaN PIN APD with much improved device performance [11, 12].



(a)



(b) Figure 3. 3D AFM images of etched mesa sidewall (a) before wet etching and (b) after wet etching. These plots were obtained with rotation angle is 85 degree and pitch angle is 10 degree.

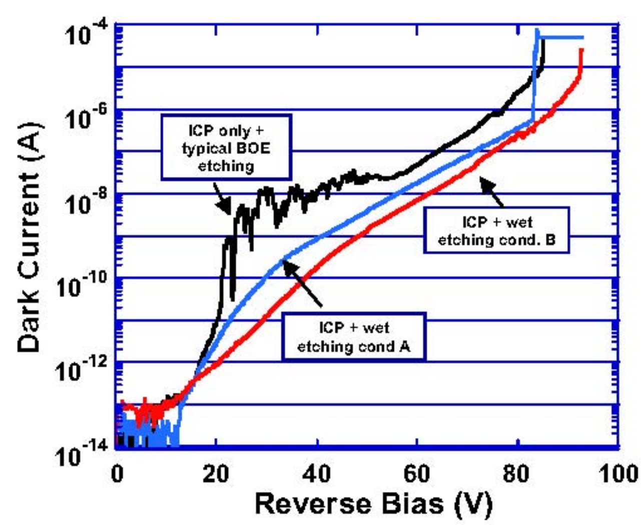


Figure 4. Reverse leakage current comparison of fabricated GaN PIN diodes grown on SiC substrate with different post-etching treatment techniques.

CONCLUSIONS

In summary, we have developed a post-dry-etching surface treatment technology for GaN minority carrier devices using a simple electrode-less UV-assisted wet etching technique. A DOE study shows that the optimal recipe consisting of a lower $K_2S_2O_8$ concentration level and a higher KOH concentration level may effectively reduce the leakage current as well as improve the surface morphology. With optimal surface treatment condition, device surface morphology and leakage current can be effectively improved and a much improved device leakage performance can be achieved.

ACKNOWLEDGEMENTS

The authors would like to thank the Ms. Bravishma Narayan for paper proof-reading, Mr. Matt Britt for technical assistance of the laboratory setup, and the staffs in Georgia Tech's Microelectronic Research Center (MiRC) for cleanroom operation support. The project is supported by the DARPA DUVAP program (Contract # FA8718-07-C0002). This paper is approved for public release and distribution unlimited.

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ACRONYMS

DOE: Design of Experiment
ICP: Inductive Coupled Plasma
RIE: Reactive Ion Etch
AFM: Atomic Force Microscope
RMS: Root Mean Square
HFET: Heterojunction Field Effect Transistors
APD: Avalanche Photodiode
PEC: Photoelectrochemical