An InGaP/GaAs HBT/JFET BiFET technology for PA bias circuit applications

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Keywords: InGaP, HBT, JFET, BiFET, integration, VVR

Abstract

This BiFET technology integrates a JFET device, also called a voltage-variable resistor (VVR) device, into the emitter layer structure of an InGaP/GaAs HBT. This new VVR device enables new PA bias circuit designs with lower or no voltage reference. This technology only requires one additional mask, one additional etch, and 2 additional epi layers as compared to an HBT-only process. These minimal changes add minimal cost to this BiFET process. The HBT device showed no appreciable performance trade-offs with the additional epi layers. Since the p-n heterojunction controls the drain current rather than a gate metal, manufacturing this device requires tight control of the InGaP emitter, GaAs channel, and InGaP etch stop layers. Doping and thickness control both across-wafer and wafer-to-wafer are needed to make the VVR a repeatable and manufacturable device.

INTRODUCTION

In recent years, several different GaAs BiFET technologies have been demonstrated in high-volume production environments. These approaches have integrated a PHEMT device below the HBT [1-3] or merged a MESFET device into the HBT emitter layers [4,5]. Adding these additional devices to an existing HBT process can add considerable complexity and cost to both the process and epitaxial layer growth.

This paper presents a BiFET technology with a JFET device integrated into the emitter layers of an HBT epi structure. First, we review the basic construction of the JFET device and its integration into an existing HBT process flow. HBT characteristics are shown to illustrate the negligible changes in HBT performance as compared to an HBT-only process. Next we show the JFET device characteristics and how this simple JFET device is useful in PA bias circuit applications. The JFET device is also referred to as a voltage variable resistor (VVR) to reflect its application. We will refer to the JFET device as a VVR device in the remainder of this paper. Finally, we present manufacturing data from the VVR device and highlight challenges faced in making this a repeatable, robust process.

PROCESS INTEGRATION OF HBT AND VVR DEVICES

This technology development sought to add a FET device to an InGaP/GaAs HBT-only process with a minimum of additional process steps and changes to the epi structure. This new VVR device enables new bias circuit designs not possible in an existing InGaP HBT-only production process. By doing so, the cost of the new technology is only slightly increased versus an HBT-only process.

These modifications to the HBT-only process and epi structure will be highlighted. Figure 1 shows the construction of both the HBT and VVR devices in this technology. The epi structure has two additional layers vs. the HBT-only process. An InGaP etch stop layer and GaAs channel layer are inserted between the InGaP emitter layer and the cap contact layers. This epi structure has been used before in HBT-only device structures without detrimental effects to HBT device performance [6]. The VVR device does not use a gate metal over the channel region but rather the p-n heterojunction to control conduction between the source and drain. The HBT base metal also serves as the backgate contact metal for the VVR device. Isolation of the source and drain mesas is formed by a wet recess etch to the InGaP etch stop layer. No gate metal deposition step is used in device formation. Source and drain contacts are formed using the same metal layers as the contacts to the HBT emitter mesa. Therefore only one additional mask layer and one additional etch step are added to the existing production InGaP HBT process flow.

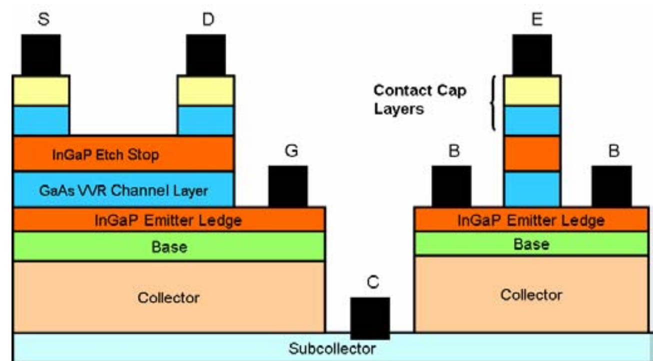

Figure 1. Device integration in this BiFET process. The VVR (JFET device) device is shown on the left and the HBT is on the right.

HBT DEVICE PERFORMANCE

An HBT device comparison between the HBT-only and BiFET processes was done to check for any performance trade-offs. All data in the subsequent plots was taken at 25ºC on a 2um x 20um emitter HBT with four fingers. Figure 2 shows the Gummel plots where beta is shown to be approximately equal up to high values of collector current. As might be expected from the two additional epi layers, the

BiFET Gummel plot indicates a higher emitter resistance. Fly-back extraction of emitter resistance yielded 0.69Ω for the BiFET process vs. 0.3Ω for the HBT-only process. Figure 3 shows the Ic-Vce curves measured from 0 to 500uA in 50uA steps. The Ic-Vce curves show little difference between the two processes.

Small signal measurements were also done on the HBTs in both processes. Figure 4 compares both Ft and Fmax at Vce=3V among the processes and shows little difference between the processes. Figure 5 illustrates the extracted Cbe differences between the two processes.

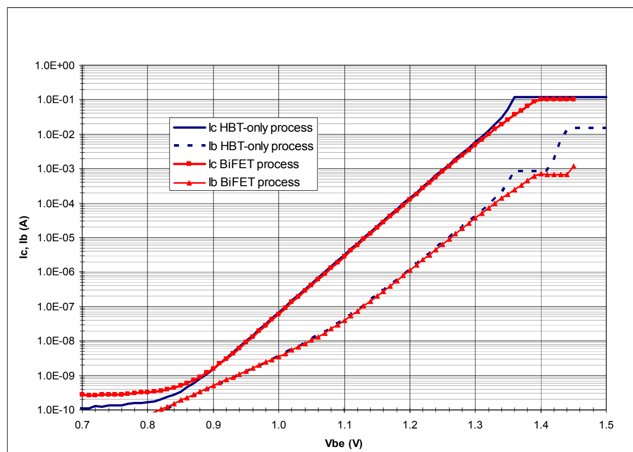

Figure 2. HBT Gummel plots comparing the HBT-only and BiFET processes

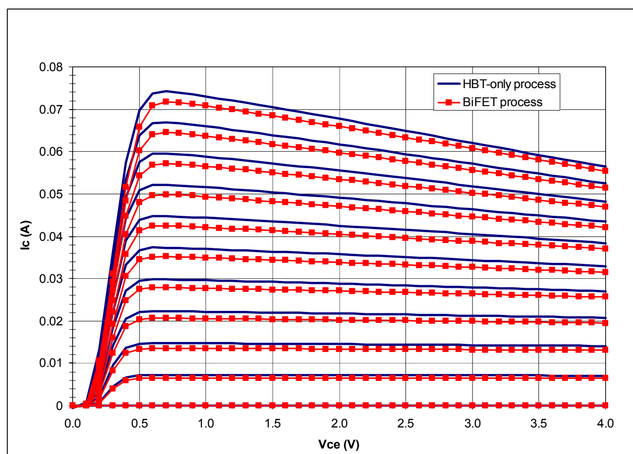

Figure 3. HBT Ic-Vce curves comparing the HBT-only and BiFET processes.

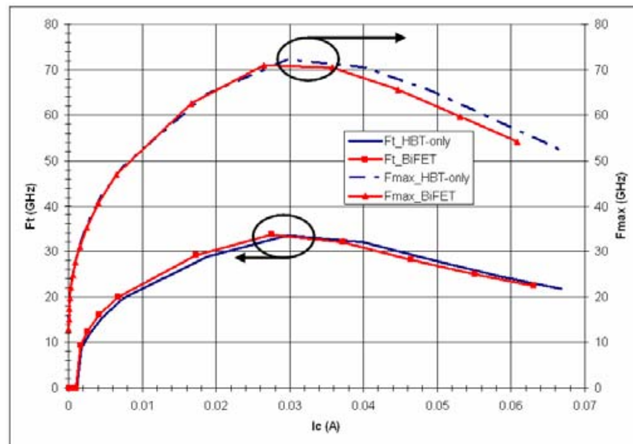

Figure 4. Ft and Fmax vs. Ic comparing the HBT-only and BiFET processes. Data was taken at Vce=3V.

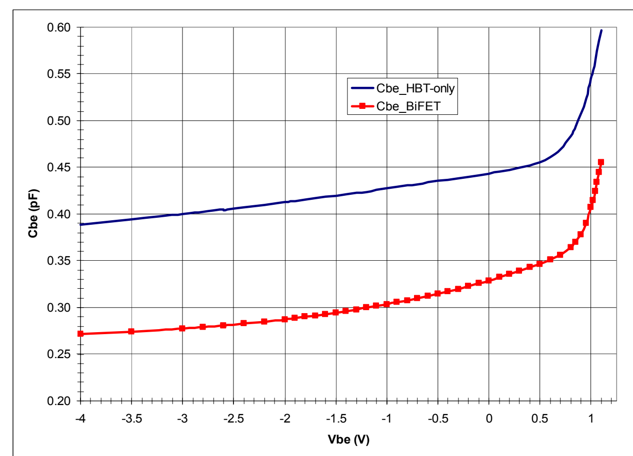

Figure 5. Extracted Cbe comparing the HBT-only and BiFET processes.

VVR DEVICE CHARACTERISTICS AND APPLICATION

The VVR device in this BiFET integration approach enables bias circuit topologies that can be operated with a lower voltage reference (Vref) or no voltage reference when compared to circuits from an HBT-only process. To illustrate how the VVR device is used, Id-Vgs and Id-Vds dc characteristics at 25ºC are shown in Figures 6 and 7. Figure 6 also illustrates an arbitrary load-line superimposed on the VVR Id-Vds characteristics. As shown by points A, A1 and A2 in Figures 6 and 7, the amount of drain current flowing in this VVR device in the “off” state is about 0.7uA/mm. When the device sees higher Vds values greater than 4V, this leakage current must be kept low to avoid undesirable currents in the bias circuit. The process and epi structure have been optimized to keep this off-state leakage current to a minimum. As seen in Figure 8, the drain leakage current at Vds=5V correlates well to the device pinch-off voltage.

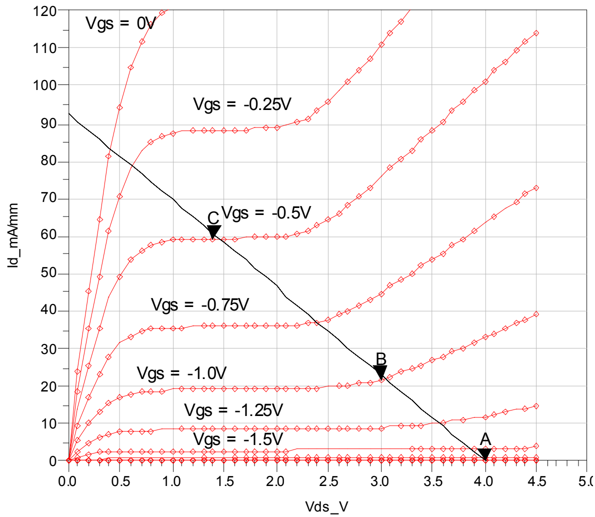

Figure 6. Id-Vds VVR measurements at T=25C. Points A, B and C shown along load-line.

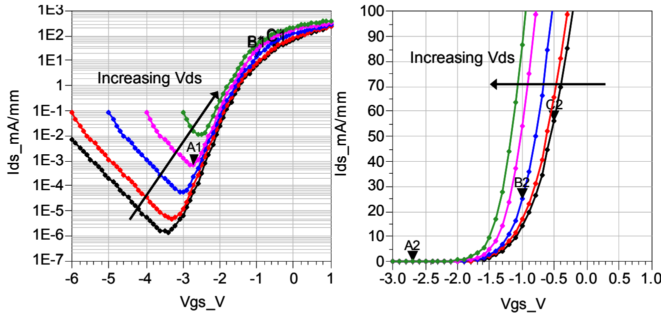

Figure 7. Id-Vgs measurements in logarithmic and linear scale. Vds values were 1.5, 2.0, 3.0, 4.0, and 5.0V.

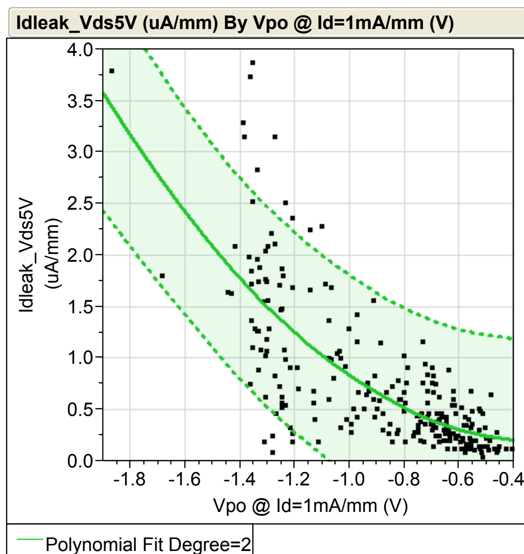

Figure 8. The Id minimum at Vds= 5V vs. pinch-off voltage, Vpo, at Id=1mA/mm from Ids-Vgs measurements.

Modeling of the VVR device has also been done using a modified PHEMT model. Figure 9 shows Ids vs. Vgs at Vds=2V measured vs. modeled data over temperature. Figure 10 shows Igs vs. Vgs at Vds=2V measured vs. modeled data over temperature. Not shown is the model fit for Ids vs. Vgs and Igs vs. Vgs over higher values of Vds.

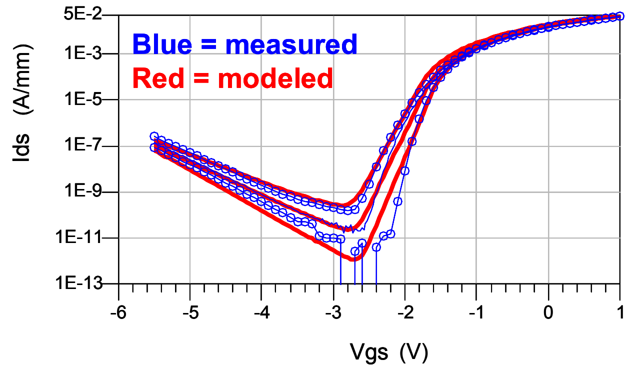

Figure 9. Ids-Vgs measured vs. modeled data over temperature (-30, 25, 85ºC) at Vds = 2.0V.

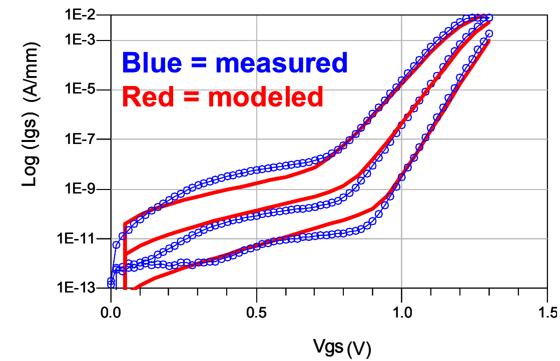

Figure 10. Igs-Vgs measured vs. modeled data over temperature (-30, 25, 85ºC) at Vds = 2.0V.

VVR DEVICE MANUFACTURING

This VVR device is a JFET where conduction in the channel is controlled by the underlying p-n heterojunction. Since no gate metal is present above the channel, the VVR device manufacturability is heavily dependent on the epi layer uniformity across-wafer and targeting run-to-run. Figure 12 shows the across-wafer variability in the pinch off voltage, Vpo, extracted at Id = 1mA/mm on a 100 mm diameter wafer. Figure 12 shows a trend chart for the same Vpo metric for one-hundred 100mm wafers processed from 3 epi batches of the same structure. This trend shows that epi targeting is crucial for manufacturability.

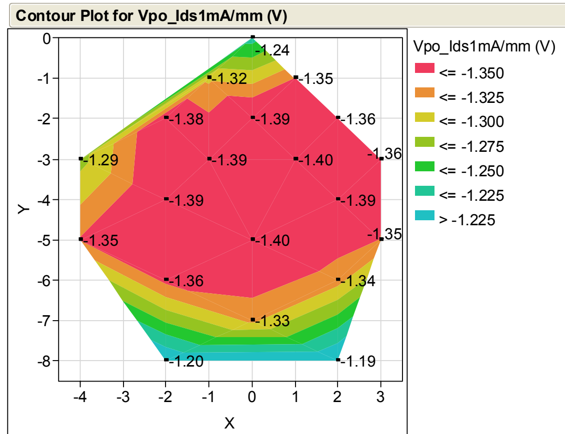

Figure 11. Wafer map of pinch-off voltage Vpo at Id of 1mA/mm showing radial variation on a 100mm wafer.

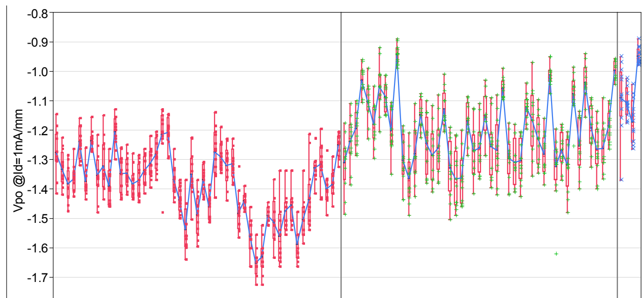

Figure 12. Trend chart pinch-off voltage Vpo at Id = 1mA/mm for 100 wafers. All wafers have the same epi structure. Marker colors represent epi batches.

Conclusions

A BiFET technology that integrates a VVR device into the emitter layer structure of an InGaP/GaAs HBT has been developed. This technology enables PA bias circuit designs that are not possible in an HBT-only process. This technology only requires one additional mask, one additional etch, and two additional epi layers as compared to an HBT-only process. The minimal process and epi changes add minimal cost to the BiFET process. The HBT device showed no appreciable trade-offs with the additional epi layers. Since the p-n heterojunction controls the drain current rather than a gate metal, manufacturing this device requires tight control of the emitter epi layers.

Acknowledgements

The authors would like to thank D. Limanto and J. Fendrich for taking most of the measurement data. The authors would also like to thank the processing engineering technicians for their help, particularly K. Scott and C. Duke.

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Acronyms

InGaP: Indium Gallium Phosphide
HBT: Heterojunction Bipolar Transistor
JFET: Junction Field Effect Transistor
BiFET: Integrated HBT and FET devices
VVR: Voltage Variable Resistor
PA: Power amplifier