The Development of a Symbolically Defined Large Signal InP/GaAsSb Type-II DHBT Model for 200 GHz Mixed Signal Circuit Simulation

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Abstract

A large signal device model is developed for type-II InP/GaAsSb/InP devices that is based on the UIUC Type-I SDD model. The model accurately characterizes a balanced 480/420 GHz f_T/f_{MAX} device, and is used to design and simulate a 200 GHz static frequency divider.

INTRODUCTION

Type-II InP/GaAsSb devices have been fabricated at the University of Illinois with cutoff frequencies (f_T) of over 630 GHz and balanced f_T/f_{MAX} of 480/420 GHz, all with a breakdown of over 3 volts [1]. Given their impressive frequency performance and breakdown voltage, type-II DHBTs are poised to be a major player in microwave and high frequency mixed signal circuits as operational frequencies approach the terahertz band.

In order to precisely design these nonlinear microwave and mixed-signal circuits, an accurate large signal model is required. The current industry standard model, the Vertical Bipolar Inter-Company (VBIC) model, was developed for silicon homojunction BJTs and therefore is incapable of properly modeling the physics of modern DHBT devices. The model lacks equations to properly model the properties of the heterojunctions at both the BE and BC interface, leading to significant linearity prediction errors [2]. The Agilent HBT model is another popular model in industry, but (to the author's knowledge) its type-II DHBT modeling ability has never been specifically shown in literature.

In this paper the UIUC SDD Type-II model, a large signal InP/GaAsSb type-II model developed at the University of Illinois, is presented. The model is implemented as a symbolically defined device in Agilent's Advanced Design System (ADS), and is based on the well established UIUC SDD type-I InP/InGaAs model, but has been altered to model the different charge transport phenomena that occur in type-II devices. The model is extracted for a balanced f_T/f_{MAX} type-II device fabricated at the University of Illinois and is capable of giving an excellent fit to both measured DC and RF data across the entire bias range of the device. The UIUC SDD Type-II model has been tested in high frequency mixed signal circuit simulations, through the design and simulation of a 200 GHz static frequency divider, which will be described in the paper.

MODEL OVERVIEW

Type-II DHBTs, have charge transfer characteristics that are significantly different than their type-I counterparts due to the relative position of the base conduction and valence band. Typical band alignments for type-I and type-II DHBTs are shown in figure 1 below. Injection of carriers from the emitter to the base is totally thermionic since there is no conduction band spike at the BE

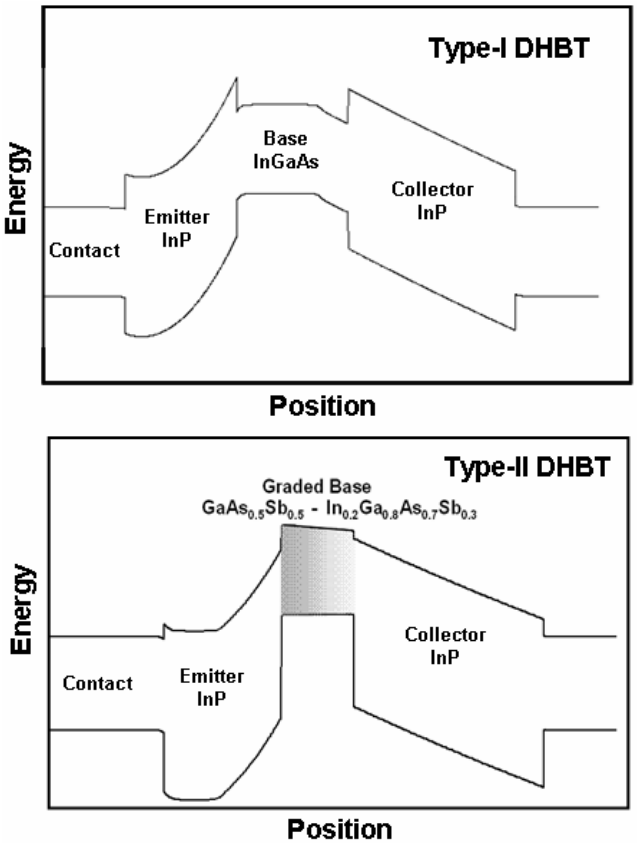

Figure 1: Type-I and Type-II DHBT Band Structures

junction, as in type-I alignment, leading to type-II device having longer base transit times than type-I devices. Type-II devices however have a desirable base-collector offset that allows minority carriers in the base to be energetically injected into the collector. The type-I base-collector barrier blocks current injection into the base, giving type-I devices poorer linearity due to the DC current blocking effect and longer collector transient times.

The UIUC SDD Type-II model is based upon the UIUC SDD Type-I model [3], which at its core is based on the traditional Gummel-Poon integral charge control relation [4]. This relation has been modified in this type-II model to account for the thermionic transfer of carriers from both the emitter and the collector into the base by the incorporation of Richardson thermionic emission voltage-current relationship:

$$J = A^{*}T^{2}\exp(-\frac{q\phi_B}{kT})\left[\exp(\frac{qV}{nkT})-1\right] \quad (1)$$

where ϕ_B is the barrier potential and A^{*} is the effective Richardson coefficient [5]. In addition, the base-emitter diffusion capacitance is increased and collector transient times are decreased to account for slower base and faster collector carrier velocities. The complexity of the UIUC SDD Type-I heterointerface current blocking modeling parameters [3] are reduced to account for the reduced, but not eliminated current blocking that occurs at the base-collector junction [6].

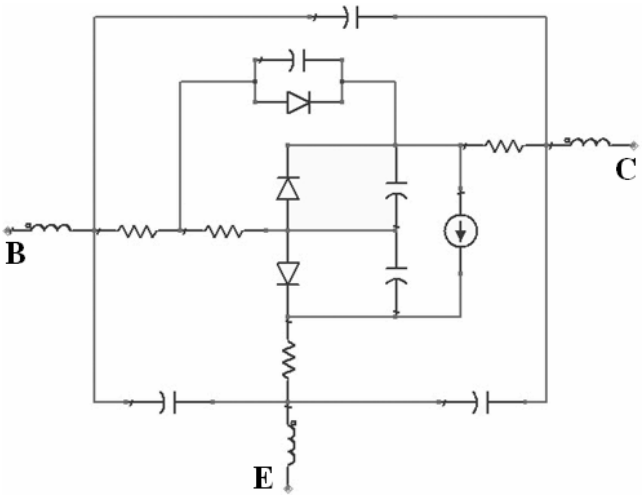

Figure 2: UIUC SDD Type-II Model Topology

The overall model topology is identical to the UIUC SDD Type-I model, as is seen in figure 2 [2]. The model has three levels: intrinsic, extrinsic, and parasitic. The model topology is developed for a standard mesa based heterojunction process. Working from the outside in, the model incorporates the parasitic capacitances and inductances of the short lengths transmission line contacts to the device that cannot be calibrated out, the extrinsic base-collector junction along with its associated capacitance, and extrinsic resistances and capacitances associated with the physical separation of these areas in a device layout. The parallel diodes, capacitor, and current source model the intrinsic device (the portion of the HBT directly beneath the emitter). It is here that the core type-II modeling is embedded.

MODEL VERIFICATION

Three means of verifying the modeling ability of the UIUC SDD Type-II model are presented. Measurements were taken of device DC current and voltage families, forward Gummel characteristics, and extrapolated unilateral current gain frequency (f_T) versus Ic bias. Each of these measurements was used to extract the parameters of the model, and when compared to the modeled values, gives an indication of the modeling accuracy.

All DC measurements were taken using an HP4142B DC source monitor unit. Figure 3 shows the measured and modeled collector current versus collector-emitter voltage and base-emitter voltage versus collector-emitter voltage for a base current from 0 to 240 uA. From the Ic vs. Vce plot we can see that the model is extremely capable of modeling the DC large signal characteristics of the device. It properly models the device collector-emitter turn on voltage and knee effects, while showing slightly too

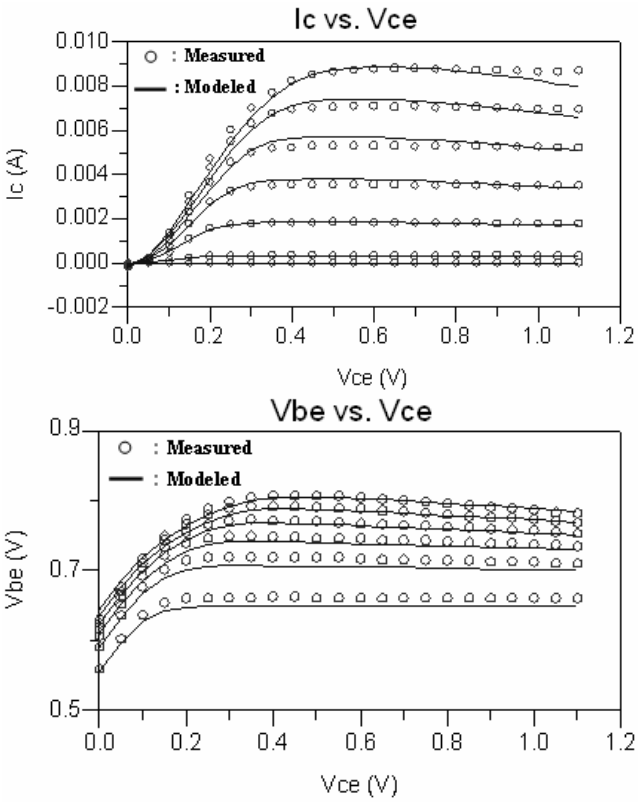

Figure 3: DC Current and Voltage Families of Device (Ib = 0 – 240 uA)

much Vce/Ic NDR at high currents caused by a slight over modeling of the thermal resistance of the device. The Vbe vs. Vce measurement is used as a metric to determine the accuracy at which the model models base current injection across all bias points. At high base current injection, the model accurately calculates the increased hole leakage into the emitter due to increase in device temperature, which shows itself as a roll off of the Vbe vs. Vce curve.

Comparisons of the measured and modeled forward Gummel characteristics of the device (Fig. 4) show that the model correctly models both minority and majority charge injection across the base-emitter junction. This device has a very large Ic-Ib crossover voltage, which is believed to be due to a slight connection between the base and emitter metals. The UIUC SDD Type-II model is still able to model this with the addition of an additional leakage current path around the junction.

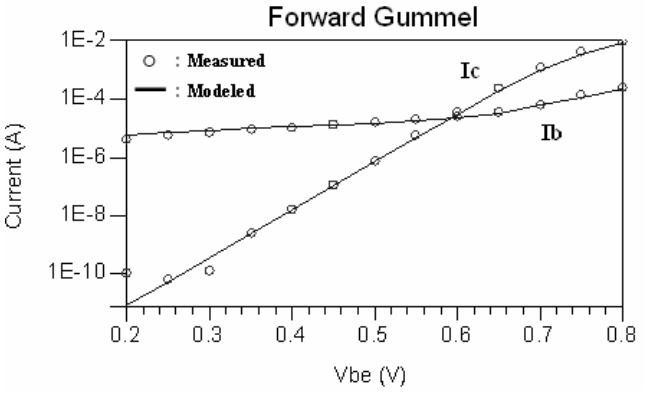

Figure 4: Forward Gummel Characteristics of Device

The S-parameters of the device were measured from 500 MHz to 50 GHz with an Agilent 8364A Parameter Network Analyzer (PNA). From the S-parameters, the unity current gain frequency (f_T) of the device was determined by extrapolating the magnitude of h_{21} at a slope of 20 dB/decade to 0 dB. The measured (extrapolated) values of f_T are used as the main assessment of the model's small signal RF modeling ability. Figure 5 shows a comparison between the measured and modeled f_T versus Ic bias. Each locus of points represents a constant collector-emitter voltage, with Ib being swept from 0 to 240 uA. The model gives a good representation of the device RF characteristics.

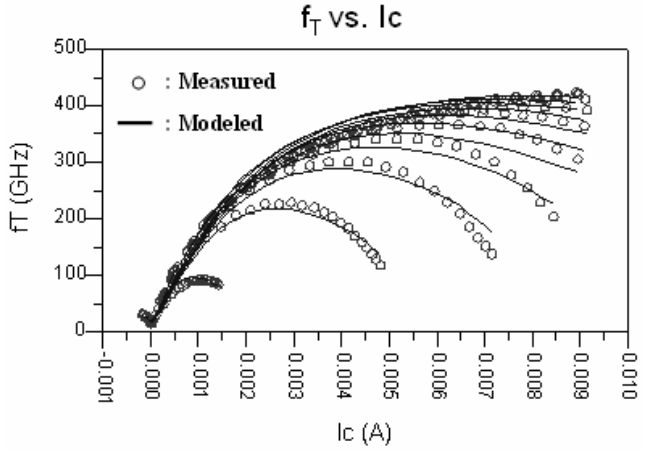

Figure 5: f_T versus Collector Current

MIXED SIGNAL CIRCUIT DESIGN

As verification that this device model will work properly and give the expected results in high frequency mixed-signal circuit design, the UIUC SDD Type-II model is used to design a divide by two static frequency divider. Static frequency dividers are a common mixed-signal circuit, and are often used to benchmark a new technology or process because they give a clear indication of how fast the given devices can operate in a tightly integrated mixed-signal design where typical metrics like f_T and f_{MAX} are not as relevant. They are also commonly used in the feedback path of phase-lock loops to facilitate high frequency synthesis, since they are capable of providing frequency division across a broad bandwidth.

A static frequency divider is essentially a flip-flop with negative feedback between its output and input so that the output transitions every time the clock signal transitions twice, providing an output signal whose fundamental frequency component is half that of the input clock signal. A schematic showing the basic operating principles of the divider is shown in figure 6. When operated at high frequencies, the input and output device impedances tend to filter all but the fundamental component of the signal, giving practically sinusoidal signals.

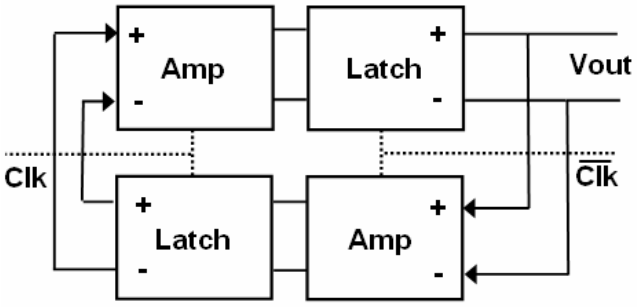

Figure 6: Block Diagram of Static Frequency Divider

This design is implemented in emitter coupled logic (ECL) because this logic style it is extremely fast and well suited to NpN DHBTs. ECL circuits are capable of operating at very high frequencies due to the fact that ideally all of the devices in the circuit will remain in the forward-active mode of operation at all times. In the forward active mode the base-collector junction is reversed bias, which results in short collector transit times and a low intrinsic base-collector capacitance. Reduced transit times and capacitances allow transistors to charge and be charged rapidly [7].

The core design consists of two identical amp/latch pairs as shown below in figure 7. A differential input clock signal drives a differential pair that essentially routes current between the amplifier stage and the latching stage. When the amplifier is active, it amplifies its differential input and charges the inactive latch to create a seed voltage. When the latch is activated, this seed voltage is amplified and latched by positive feedback through the emitter follower stage. Peaking inductors are used at the amplifier load in an attempt to cancel out capacitance, effectively put a zero in transfer function, to increase the bandwidth of this circuit.

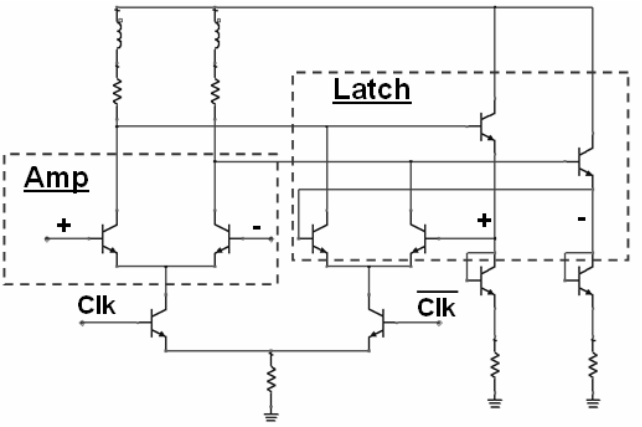

Figure 7: Circuit Implementation of Static Frequency Divider Latch, One Half of Core Circuit

The circuit, based off of the UIUC SDD Type-II model, simulates nicely in an Agilent ADS transient simulation with sinusoidal or square clock inputs. It has no convergence issues, and simulates in less than a minute on a conventional 2.5 GHz PC.

The circuit was simulated from 50 GHz to 205 GHz, the maximum frequency at which it has the proper operation. Correct circuit operation and simulation convergence is seen at all frequencies in this range. The input 'clk' and output voltage waveforms are shown for an input frequency of 205 GHz in figure 8 below.

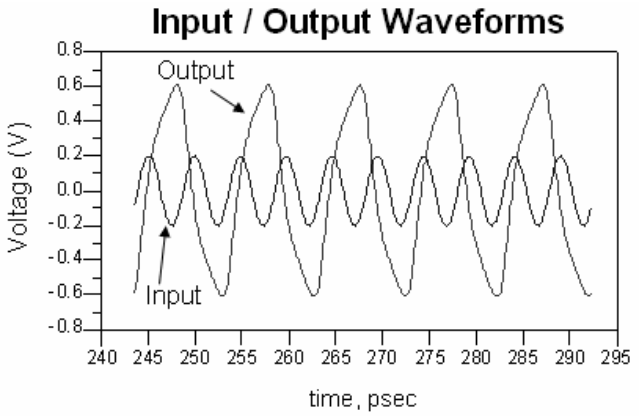

Figure 8: Simulated Input and Output Waveforms

Parasitic interconnect capacitances are not taken into account in this simulation. Layout extractions carried out in Cadence indicate that line to line capacitance and line to ground capacitance would decrease the maximum operating frequency to around 170 to 180 GHz.

CONCLUSION

In this paper, a new large-signal type-II DHBT model, the UIUC SDD Type-II model, has been presented. Being specifically developed for type-II DHBTs, it is shown to accurately characterize the DC and RF operation of a balance 480/420 GHz f_T/f_{MAX} type-II DHBT. In addition to modeling singular device, the model was used to design and simulate a static frequency divider with a simulated maximum operating frequency of 205 GHz.

ACKNOWLEDGEMENTS

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ACRONYMS

HBT: Heterojunction Bipolar Transistor
f_T: Unity Current Gain Frequency
f_{MAX}: Maximum Frequency of Oscillation
ECL: Emitter Coupled Logic
NDR: Negative Differential Resistance
SDD: Symbolically Defined Device
h_{21}: Two-Port Current Gain