

Thermal-Mechanical Characterization of Wafer Level Packaging Technologies

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Keywords: 3-D Integration, 3-D Heat Pipes, Heat Removal, Thermal-Mechanical Integrity

Abstract: 3-D passive thin film resistor heat removal test structures were fabricated on multi-layer wafer configurations to characterize and optimize vertical and horizontal heat removal in wafer level packaging technologies. Four layer heat removal test coupons with optimized thermal management design demonstrate a thermal resistance of less than 36°C/W. Two layer test cells with DC interconnections and active device structures were also fabricated to evaluate and characterize the thermal-mechanical integrity for 3-D integrated structures. The robust multiple layer construction demonstrates no measurable changes in DC resistance of interconnects or small signal performance of active devices after completing 10 thermal stress cycles from -55 to 125°C. Results from 3-D x-ray computed tomography imaging will be presented to demonstrate advanced thermal-electrical-mechanical integrity analysis for multilayer structures.

Introduction:

Advancements in 3-D packaging for compound semiconductor technologies have opened new frontiers for integrating RF circuits at wafer and chip levels. Integrating circuits layers intimately with down to microns of separation along the z-direction and $\lambda/2$ cell spacing in x-y directions allows for the realization of compact and light weight multifunctional circuits to meet emerging requirements for future space and military-defense systems. The development of 3-D heat removal methods must be addressed to ensure that advancement in circuit integration via packaging technologies will not compromise device performance and allow for reliable circuit operation.

Key challenges for thermal management of multilayer 3-D circuits include the need for developing high heat removal methods to accommodate heat generation within tight space allocations. High heat removal methods directly beneath active devices in upper layers of a stack are necessary to reduce the temperature rise in active layers. In this work, passive thermal management approaches compatible with microelectronic device circuit fabrication were investigated using TFR-based test structures for a quick turn around

design-fabrication-test process to develop vertical and horizontal heat removal method for 3-D integrated circuits.

Experimental:

An illustration of the thermal test cell and experimental test set up used to characterize vertical and horizontal heat removal in the multilayer construction is provided in Figure 1. In this work, 100 mm diameter GaAs substrates with thickness ranging from 25 to 2 mil were assembled together in a vertical configuration. NiCr Thin Film Resistors (TFRs) were fabricated to serve as heaters in the multilayer test structures. The heaters were placed in spatial configurations to emulate heat loads of devices. The dimensions for the TFR heaters used in this work ranged from (L x W) 120 x 25 to 20 x 50 μm^2 to resemble DC heat dissipation under nominal operating conditions.

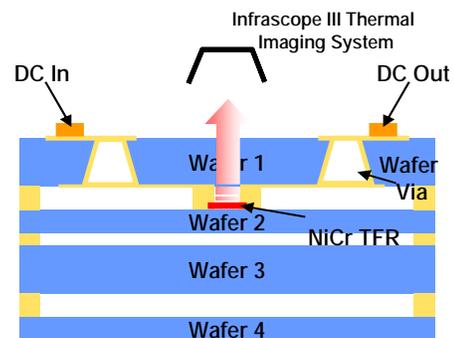


Figure 1. Illustration of 4 layer thermal test structures employed to characterize vertical and horizontal heat flow in the 3-D multilayer construction.

Multilayer thermal test cells with and without the heat removal pipes were fabricated to characterize optimal vertical and horizontal heat removal methods. Temperature measurements for the multilayer thermal test cells were obtained with a QFI Infrascopes III Thermal Imaging Microscope. Ansoft ePhysics 2.0 finite element analysis software was used to simulate the temperature rise in the multilayer configuration. IR thermal imaging results from the multilayer test structures were compared to FEA thermal simulations to calibrate the thermal conductivities of vertical

and horizontal heat removal design features employed in the thermal test structures to reduce the peak temperature rise in the top layers of the multi-layer construction.

Two layer test structures with active devices were fabricated to characterize the thermal-mechanical-electrical integrity of the multilayer structures. DC and s-parameter measurements were performed on interconnect chains and active devices respectively. The measurements were performed during multiple stages of the integrity analysis process, including on wafer, after dicing, and after thermal stress cycling from -55 to 125°C using 5°C/min heating and cooling rates with 10 minute dwell times at each end point. Illustration of the two layer thermal stress cell is shown in Figure 2.

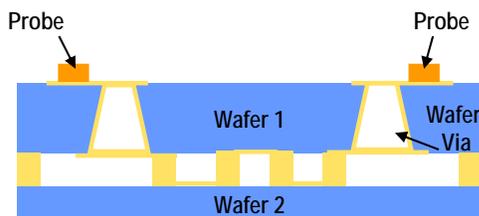


Figure 2. Illustration of 2-layer thermal-mechanical integrity test structures employed to characterize robustness of multilayer structures.

An advanced x-ray computed tomography 3-D imaging technique was developed to provide nondestructive physical analysis methods for rapid feedback to optimize heat pipe performance. The high resolution x-ray imaging technique provides characterization of ICIC alignment between adjacent layers and cavity height measurements. The x-ray imaging technique was also used to investigate changes in mechanical integrity of the multilayer structure. X-ray imaging of the multilayer structure before and after thermal cycling was used to look for evidence of wafer cracking, ICIC breakage, and thru wafer via failure to correlate the thermal mechanical failures with electrical performance to support the development of advanced test methods and design rule guidance for the 3-D integrated structures.

Experimental Results:

The NiCr TFR heaters in Wafer 2 were biased from the top layer of the 4 layer stack to generate local heat loads in the 3-D integrated structure for 3-D heat flow analysis with IR thermal imaging.

IR thermal imaging measurements shown in Figure 3 (A) report a peak temperature rise of 31°C for the heaters in this test structure. The thermal analysis results suggest that the 3-D thermal management approach employed to vertically and horizontally remove the heat away from heat dissipating TFRs in layer 3 allows for effective heat removal and minimal temperature rise.

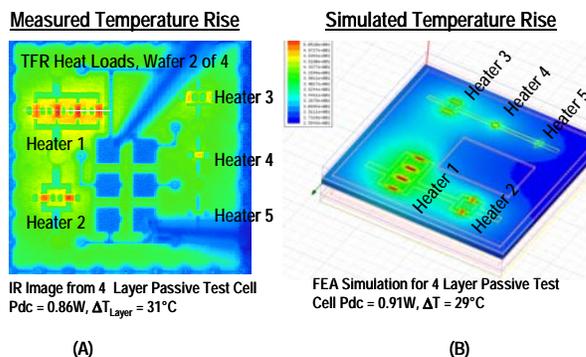


Figure 3. (A) IR thermal image of wafer 2 in the 4 layer thermal test cell stack up, (B) FEA thermal analysis results for wafer 2 in the 4 layer thermal test cell.

FEA thermal analysis was employed to characterize the vertical and horizontal heat flow through each layer. The results from thermal analysis for wafer 2 in the multilayer stack are shown in Figure 3 (B). Thermal simulations report a 29°C temperature rise. The thermal analysis results from FEA agree well with the results obtained from IR measurements. To calibrate the FEA model parameters and obtain more statistics, sixteen thermal test cell sites were measured across the 100 mm diameter multilayer structures for TFR DC power dissipations ranging from 0.2 to 1 watt. The results are summarized in Figure 4, where a 36°C/W average thermal resistance was obtained from IR thermal measurements for wafer 2 of 4 in the multilayer thermal test cell.

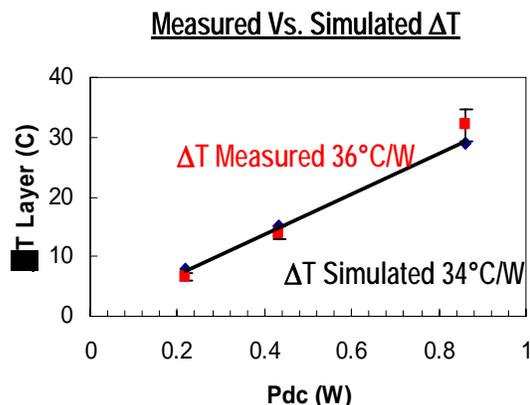


Figure 4. Measured and simulated temperature rise for wafer 2 of 4 in the multilayer thermal test cell for TFR dissipated powers ranging from 0.2 to 1 watt.

The results obtained from multiple test sites demonstrate 8% standard deviation across the 100 mm diameter 4 layer wafer stack up. The high across-wafer uniformity shows that NGST's fabrication process does not introduce large variability in performance of key heat removal features such as vertical heat pipes, metal films, and semiconductor materials. We believe that variations in backside contact

between the thermal test cell and wafer chuck attributed to the across-wafer variation in measured temperature rise. Calibration of thermal conductivities for key heat removal design structures, such as vertical heat pipes semiconductor materials used for vertical and horizontal heat spreading, respectively, were tuned in the FEA models to calibrate them with the measured results.

Results from the FEA thermal analysis with tuned parameters are shown in Figure 4. Peak temperature rise in wafer 2 of 4 reported by the FEA simulations agrees well with the measured results from IR thermal imaging to show an average thermal resistance of 34°C/W.

Four layer thermal test cells with passive TFR heaters were also fabricated without the optimized vertical and horizontal heat removal designs to further calibrate FEA thermal analysis models heat removal design features as well as to validate results. Temperature rise measurements obtained with IR thermal imaging for wafer 2 of 4 in multilayer thermal test cells with nonoptimized and optimized vertical and horizontal heat removal designs are shown in Figures 5 (A) and (B), respectively. The peak temperature rise increases 26% from 52°C to 70°C for the thermal test cell without optimized 3-D heat removal design. It's also evident from the thermal imaging that the heat flow is diminished in the multilayer stack to increase temperature across the entire chip surface area due to the increase in thermal resistance of 57°C/W for the 4 layer thermal test cell. The results from this work show that thermal imaging of multilayer test structures with TFR heaters can be used to develop a quick turn around process to characterize and optimize horizontal and vertical heat removal for compact 3-D integrated RF circuits.

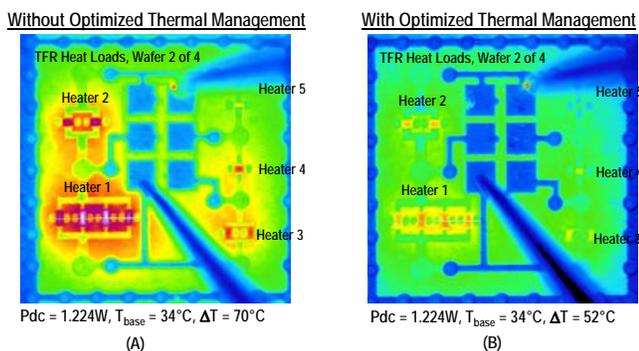


Figure 5. IR thermal image of wafer 2 in the 4 layer thermal test cell stack up (A) without optimized vertical and horizontal heat removal (B) with optimized vertical an horizontal heat removal.

Thermal-Mechanical Stress Results:

Two layer 3-D integrated test structures with active devices were screened for DC and RF functionally after dicing to select parts for thermal-mechanical stress testing. Multiple parts were thermally cycled from -55 to 125°C with 5°C/min

cooling and heating rates and 10 minute dwell times at each end point. The parts were tested at the end of 10 thermal stress cycles to screen for failures. All parts demonstrated no measurable change in interconnect DC performance and less than 1 dB change in device small signal gain S_{21} . The device small signal gain performance before and after thermal stress cycling is shown in Figure 6 for one of the nine parts. The device performance degraded less than half a dB after 10 thermal stress cycles to demonstrate robust thermal-mechanical integrity.

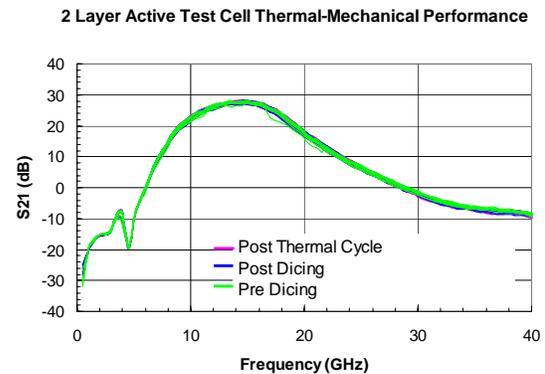


Figure 6. Small signal gain for 2 layer test cell before and after 10 thermal stress cycles from -55 to 125C with 10 minute dwell times at each end point.

X-ray Imaging Results:

Development of multilayer structures for 3-D integrated circuits introduces a new set of requirements and challenges for nondestructive metrology techniques. Advanced computed tomography x-ray imaging has been developed in this work to allow for nondestructive analysis of multilayer structures after attachment as well as to support thermal mechanical integrity analysis. Key challenges include the characterization of layer to layer alignment, wafer thickness measurements, and cavity heights analysis. X-ray imaging of a multilayer electrical test DC test cell is shown in Figure 7. The 3 microns of imaging resolution obtained with the x-ray imaging clearly resolves both wafer layers, ICIC posts, thru wafer vias, and allows for cavity height measurements of the multilayer electrical yield test structures.

2 Layer Wafer Stack High Resolution X-ray Imaging

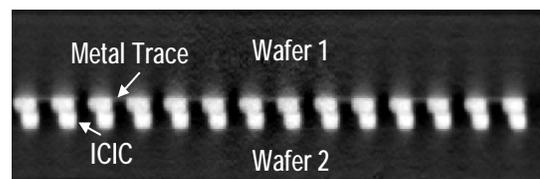


Figure 7. High resolution X-ray image of 2 layer wafer stack with DC interconnect chains.

Conclusion

Northrop Grumman Space Technology has developed a quick turn around design-fabrication-testing-analysis process to optimize horizontal and vertical heat removal methods in multilayer structures. This method has been used to advance the development of compact multilayer 3-D integrated RF circuits. The results from this work demonstrated 36 °C/W thermal resistances for 4 layer test structures with optimized horizontal and vertical heat removal design features. Two layer test structures using active devices were thermal stress cycled from -55 to 125°C. The chips demonstrate less than 1 dB change in small signal gain S_{21} after completing 10 cycles to demonstrate robust thermal mechanical integrity. Advanced computed tomography 3-D x-ray imaging technique was developed in this work to enable nondestructive analysis of multilayer 3-D integrated RF circuits.

Acknowledgements

The authors also wish to thank the entire engineering and processing team at NGST's Microelectronics Product Center for multilayer fabrication and testing.

Acronyms:

DC: Direct Current

FEA: Finite Element Analysis

ICIC: InterCavity InterConnect

IR: Infra-Red

NiCr: Nickel Chrome

QFI: Quantum Focus Instruments

RF: Radio Frequency

TFR: Thin Film Resistor