Process Development and Characteristics of Nano III-V MOSFET

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Abstract

The compound semiconductor channel materials have recently drawn great attention because of their potential to solve the upcoming Si MOSFETs scaling problem and become the next generation high-speed, low-power devices. In this work we review the latest silicon technology and report the process development of submicron III-V MOSFETs. A new approach has been demonstrated to overcome the high interface density of states between gate dielectric and channels by applying an interface-control-layer. The proposed design and results show promise for realizing compound semiconductor based MOSFETs

INTRODUCTION

For more than 30 years, Silicon-based MOSFET technologies have been advancing at a dramatic pace due to the progressive and aggressive scaling-down of MOSFET structures to smaller dimensions, resulting in improved performance. However, scaling MOSFET to and beyond the 22-nm technology node (requiring a physical gate length < 9-nm) will likely require the introduction of new materials or improvements in device structures in order to sustain the performance increases every year [1].

Among several emerging nano-devices with the potential to integrate with current silicon technology, III-V-based MOSFETs are most attractive due to their high electron motility [2]. In addition, III-V materials can be fabricated into device structures using "top-down" lithographic and etching methods, which are well-established and reliable techniques. The challenges faced by III-V MOSFET are, nevertheless, daunting due to the lack of a high quality and thermodynamically stable native oxide that eliminates interface states and Fermi level pinning. Recently, Ga_2O_3 [3] and HfO_2 [4] were used as gate dielectrics. In [4], the interface-state density (D_{it}) is in the order of $10^{12}/cm^2$-eV and $I_{on}/I_{off} \sim 10^3$. Developing a new material system is absolutely crucial to achieving a device with stable CV property and low leakage current.

In the work presented in this extended abstract, we will review the state of the art silicon MOSFETs technology, comparing silicon and compound semiconductor material systems, and propose the designs for nano III-V MOSFETs, including process development and crystal growing techniques.

OVERVIEW OF SILICON CMOS TECHNOLOGY

1) Gate dielectric: To increase drive current and reduce supply voltage, scaling dielectric thickness has long been recognized as the key to scale devices. Short channel effect can also be controlled by scaling dielectric thickness with channel length. However, thinner gate dielectric means the tunneling gate leakage current will rise. High k gate is thus introduced because it is physically thicker but electrically thinner (i.e. the same capacitance). The 45nm technology node [5] incorporates ALD-HfO_2 based dielectric with metal gate to reduce phonon-scattering-induced channel mobility degradation and keep leakage current low.

2) Junction engineering: In long channel devices, external resistance is small compared to intrinsic channel resistance. But as the gate length is scaled down, the channel resistance is significantly lower while external resistance is not scaled as dramatically. As a result, junction engineering is needed to improve extrinsic resistance, which becomes a limiting factor of device performance. In addition, optimizing source drain junction depth is important to improve short channel effect. Ion-implantation is used to form shallow source drain in both n- and p-MOSFETs. The activation annealing is critical to produce diffusionless and high concentration junctions. In 45nm-node technology, multiple spike RTA and millisecond laser annealing are applied.

ADVANTAGES AND CHALLENGES OF III-V MOSFETS

Compound semiconductors have the potential for low-power and high-speed logic because their ***high-mobility*** and ***low energy-delay product*** characteristics. Current III-V FETs like HEMTs have already shown higher unity gain cutoff frequency (f_T) and less active power than silicon NMOS of the same scaling dimension[6]. However, I_{on}/I_{off} ratio is limited by the schottky gate leakage. To get high performance devices, III-V compatible gate dielectric needs to be applied on the material systems. The major difficulty is the lack of a low density of interface states. For CMOS logic applications, high hole mobility channel

devices are needed as well. But current III-V materials show hole mobility just comparable to Si. The challenge includes improving hole-mobility in III-Vs or utilizing novel materials such as Ge.

PROCESS DEVELOPMENT

Unlike silicon, it is recognized that the formation of perfect native oxides on compound semiconductor surfaces is extremely difficult. Further, the interface between compound semiconductor and oxide degrades easily during device processes. To minimize or even eliminate these effects, a new approach of making high quality MOS structure on III-V compound semiconductors is initiated.

We propose a new approach of making high quality III-V compound semiconductor based MOS structures using an 'interface control layer' (ICL) in between the III-V semiconductor channel surface and the ex-situ deposited oxide layer has been demonstrated this quarter. Preliminary capacitance-voltage (C-V) measurement results of the atomic layer deposited (ALD) Al_2O_3 (8nm)-ICL-InGaAs:Si-InP MOS structure are encouraging which show clear inversion even after 500°C annealing (Fig. 1). The hysteresis C-V curves reflect the fact that procedures of the ex-situ ALD of Al_2O_3 on ICL are not optimized.

The C-V measurements were done after the oxide layer was deposited. The initial C-V measurements of the 8nm ALD Al_2O_3-ICL-InGaAs:Si (n=5E17cm^{-3})-InP MOS structure show clear inversion (Fig. 2). Although there exists C-V hysterisis loops in this preliminary experiment, the insertion of an ICL layer does allow the MOS to reach inversion even after 500°C annealing. With proper redesign of the ICL layer structure, high quality C-V characteristics with low interface state density and without hysterisis loops are expected. This promising approach could be an important solution to the III-V MOSFET fundamental problem.

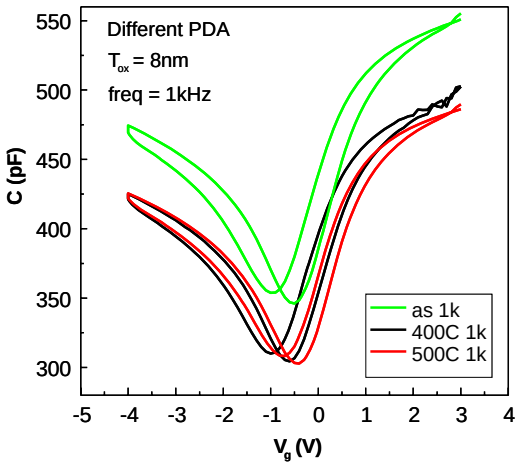

Fig 1: Quasi-static C-V curves of a 8nm Al_2O_3-ICL-InGaAs:Si-InP MOS structure measured at 1 kHz before and after annealing at 400 and 500°C.

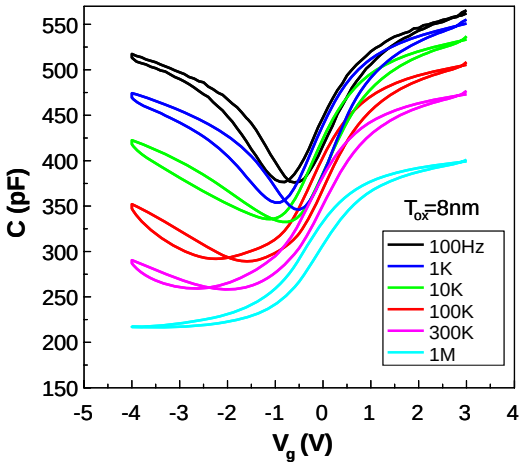

Fig 2: C-V curves of a 8nm Al_2O_3-ICL-InGaAs:Si-InP MOS structure measured 100 Hz to 1 MHz.

Another significant drawback of III-V material systems is their low tolerance to high temperature. Especially in III-V MOSFET, the non-native oxide and channel interface is degraded after thermal processes such as annealing after ion-implantation. Unfortunately, as mentioned before, in silicon industry, very high thermal budget is required to produce very shallow and non-diffusive source drain extension. This is unlikely to apply to compound semiconductors. Accordingly, we try to regrow source and drain to achieve the high-doping concentration and avoid high-temperature process steps.

We first try to regrow GaAs on samples patterned with metal deposition and dry or wet etching of the GaAs. After these processes, GaAs is re-grown by using gas source molecular beam epitaxy (GSMBE). The main target is trying to generate some growth selectivity between metal and GaAs surfaces, through adjusting growth parameters, such as substrate temperature, V/III ratio, and growth rate. Before loading into the MBE system, the patterned sample is cleaned with the following flow: acetone (3min)->methanol (3min)->IPA (3min) -> GaAs etching (1min). The appropriate cleaning process is extremely important for regrowth, because a dirty GaAs surface will be difficult to be desorbed perfectly, and this will lead to rough surface after the re-growth of GaAs.

The regrowth starts with surface oxide desorption, which heats the sample up under arsine (AsH_3) over-pressure. If the sample is well cleaned, a typical 2x4 RHEED pattern can be observed when the surface oxide is desorbed. After oxide desorption, growth parameters are set to desired values and the growth of GaAs will start.

To achieve selective growth, usually the substrate temperature is elevated higher than oxide desorption temperature to offer Ga atoms more energy to migrate. Also the V/III ratio is set as low as possible to decrease the chance of the combination of Ga and As. However, several different conditions have been tried up to now and no

selective growth can be achieved. The GaAs grown on metal surface, which can be seen Fig.(3)-(b) and Fig.(3)-(d), still forms poly-crystal. Lowering the growth rate further or increasing substrate temperature may help to approach the selective growth. If selective growth can not be done in the current MBE system, the removal of poly-GaAs would be an issue to solve. Another issue of the regrowth is the change of etched GaAs profile. From Fig.(3)-(c) and Fig.(3)-(d), it can be seen that the profile of GaAs surface became smoother after the regrowth. The change in profile may be due to the migration of original GaAs under high temperature. This profile change may increase difficulties in extending regrown material underneath the gate oxide, which is expected to be done with regrowth.

The other topic in the future includes the re-growth of other arsenic compounds, such as InGaAs or InAs for better conductivity and ohmic contact. Also, the interface between original and re-grown materials may affect the characteristics of the device.

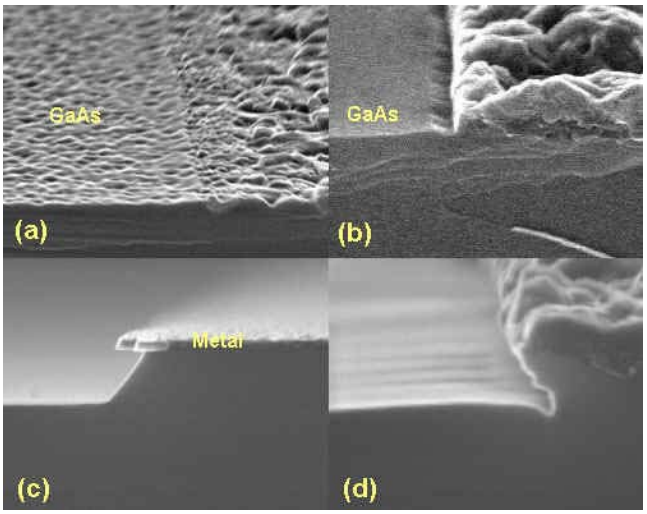

Fig 3: (a) Re-grown GaAs sample without proper cleaning. (b) Smooth re-grown GaAs surface, which is cleaned with the flow mentioned in the article. (c) Patterned GaAs with under cut (before regrowth). (d) The side profile of the re-grown sample

Finally, Sub-100nm self-aligned gate process for high-speed MOSFET fabrication has been demonstrated. Using a tri-layer photoresist structure, the 50nm T-gate structure (Fig. 4) is achieved. The tri-layer photoresist structure for the T-gate process consists of a bottom layer that defines the gate footprint, a top layer that forms the gate top, and a middle layer that forms an overhanging lip to ensure lift-off.

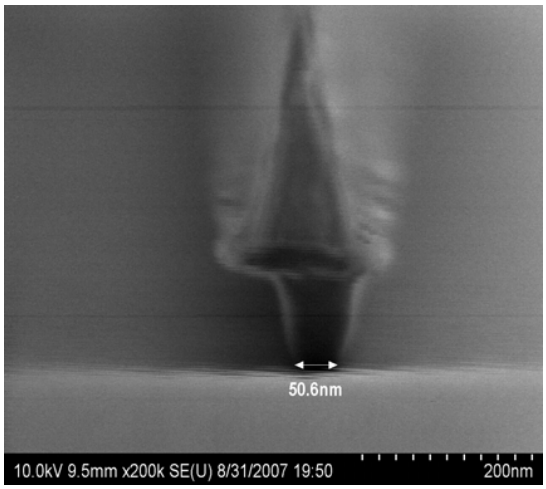

Fig 4: SEM picture of the fabricated T-gate with a 50 nm gate-length.

CONCLUSIONS

This work has demonstrated use of interface control layer with regrowth technology to complete submicron III-V channel MOSFETs. The incorporation of ICL structure should be able to overcome the oxide III-V semiconductor interface problems. To prevent the compound semiconductor material degradation from heat treatment such as thermal annealing, source and drain regions are formed by re-growth process inside a MBE system instead of using ion-implantation.

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ACRONYMS

MBE: Molecular Beam Exipaxy
MOSFET: Metal-Oxide-Semiconductor Field Effect Transistor
PDA: Post Deposition Annealing
ALD: Atomic Layer Deposition