Novel GaAs Switch for Compact and Efficient Power Conversion

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Abstract

The development and demonstration of a novel GaAs switch called Substrate-Driven FET (SD-FET) is reported in this paper. The SD-FET process is compatible with standard large volume pHEMT processes and the device has far superior switching properties compared to state-of-the-art Si devices. This combination of cost effectiveness and excellent performance makes the SD-FET vital for meeting the challenging power requirements of next generation portable applications. Devices with current capability of 20A with a gate width of 1 meter, specific on-resistance of 0.26mΩ-cm^2, and turn-on and turn-off transitions less than 1nsec have been demonstrated. Power losses due to conduction, gate charge, output capacitance and switching transitions are lower than that of commercially available state-of-the-art Si devices, thereby validating the capability of the SD-FET in enabling compact and highly efficient power conversion. The performance of the SD-FET in a multiphase buck converter application was analyzed showing at least 9 percentage points improvement in efficiency over an equivalently rated Si-based counterpart.

INTRODUCTION

Consumers of portable electronics want feature-rich, smaller and easy to carry devices, without compromising battery life. Aggressive CMOS scaling enables ICs that meet the growing demand for increased system functionality. However, these ICs are increasingly power hungry resulting in challenging metrics being imposed on efficiency, power density and transient response of the power converters that drive these systems.

High efficiency is the principal requirement to maintain, if not increase, battery life. High power density is driven by the small form factor associated with portable devices and the multiplicity of power conversion needs in a given system. Faster transient response is required to support functionality.

State-of-the-art power converters employing Si FETs are usually operable at switching frequencies only up to several 100kHz due, at least in part, to the slower switching speeds of the Si FETs. Higher switching frequencies in the MHz range are required to reduce the size of passive elements and achieve faster transient response. A power converter with higher efficiency, in addition to preserving battery life, requires smaller heat sinks and provides cooler system operation. To this end, the power switching device, capable of operating at MHz frequencies, is a critical first step to the realization of high efficiency, high power density power converters for next generation portable applications.

Previous attempts to fabricate a high performance GaAs switch have proven to be challenging. These attempts included a buried gate with epitaxial overgrowth [1], or implanted gate [2, 3], and demonstrated high channel and gate resistance per unit die area. Additionally, the devices did not include an intrinsic body diode required in power conversion applications. Moreover, prior attempts employ structures that significantly increase die cost. Consequently, the resulting higher cost and poor performance have led to limited marketability in view of the presently available, optimized and cost effective Si-based technology.

With the application in mind, we have developed and demonstrated a novel GaAs pHEMT-based device technology called Substrate-driven FET (SD-FET). The SD-FET has superior switching properties compared to state-of-the-art Si devices. This makes

the SD-FET very attractive, if not essential, to meet the demanding power requirements of next generation portable applications. In this paper we will describe the device structure, the cost effective fabrication process and the measured device performance.

DEVICE STRUCTURE AND FABRICATION

The SD-FET device structure is schematically shown in Fig. 1. This novel device uses conductive n+ substrates for low on-resistance, power recess for high blocking voltage, interdigitated gates to reduce device footprint and lower gate resistance, large source and drain contacts, and a source trench. The source trench, shown in Fig. 2, is an interconnect that connects the lateral channel to the underlying conductive substrate and the large area source contact to provide low resistance coupling desirable for high current, switching power devices. The device also includes a monolithically integrated anti-parallel diode that provides a conductive path from source (substrate) to drain when the device is turned off. This is a critically essential device feature in power switching applications. In addition, the intrinsic anti-parallel diode does not occupy additional die area beyond the essential SD-FET device area, hence does not add to the device cost.

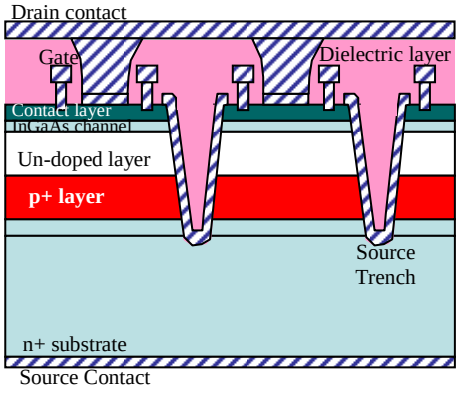

Fig. l. Schematic of SD-FET device cross-section

Most notably the SD-FET takes full advantage of well established pHEMT processes, as well as the superior material properties of GaAs over Si. Because the SD-FET process is fully compatible with standard, large volume pHEMT manufacturing processes, it is more cost effective than previously reported solutions thus addressing the challenges to date related to large volume GaAs switch manufacturing.

The starting material is a 4-inch n+ GaAs substrate with doping concentration >1×10^{18} cm^{-3}. n+ GaAs buffer layer with doping concentration of 1×10^{19} cm^{-3} is grown followed by 1000Å of $2\times10^{19}cm^{-3}$ carbon doped p+ GaAs layer, and 9000Å of $1\times10^{16}cm^{-3}$ carbon doped p- GaAs layer. The p-doped layers in conjunction with preceding n-layers form the intrinsic anti-parallel diode. Then AlGaAs/GaAs super lattice layers are grown, followed by $Al_{0.2}Ga_{0.8}As$ bottom barrier layer with Si delta-doping (1×10^{12} cm^{-2}), $In_{0.2}Ga_{0.8}As$ channel, $Al_{0.2}Ga_{0.8}As$ top barrier layer with Si delta-doping (4.5×10^{12} cm^{-2}), lightly doped wide recess GaAs layer, AlAs etch-stop layer for selective etching of first recess, and n+ GaAs contact layer.

The SD-FET fabrication process starts with device isolation by oxygen ion implantation (dose 5×10^{12}~1×10^{13} cm^{-2}), followed by the definition of the source trench by photolithography and etching using a chlorine-based inductive coupled plasma (ICP) etching process. Once the source trench is defined, AuGe/Ni/Au alloy is evaporated and lifted simultaneously in the source trench and on the n+ GaAs forming the source and drain ohmic contacts respectively. The waterless liftoff of AuGe/Ni/Au in the source trench is done in such a way where the ohmic metal covers the bottom and the top of the trench, as well as partially covering the trench side wall, as shown in Fig. 2. Subsequently thick gold is plated in the source trench to provide low resistance interconnect from the top source contact to the conductive substrate. Because the SD-FET is formed on a conductive substrate, conductive substrate was used as a plating seed layer. The source trench contributes to lower device resistance and less current crowding due to its large contact area and direct contact to the conductive substrate.

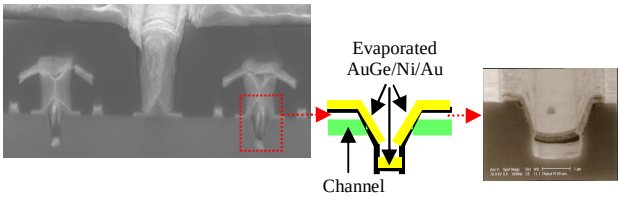

Fig. 2. Source trench formation

After source trench and drain contact formation, the rest of the process is very similar to that of a standard pHEMT. Wide recess is defined by a selective chlorine-based reactive ion etching (RIE) stopping on AlAs. AlAs etch stop is selectively wet etched using HCl based wet etchant. Gate recess is defined using a low-damage chlorine-based selective

RIE stopping on $Al_{0.2}Ga_{0.8}As$. The 0.5um gate is defined by image reversal photolithography and e-beam evaporation of 0.5um Ti/Pt/Au. Once the gate is defined, gate passivation is achieved by plasma enhanced chemical vapor deposition (PECVD) of silicon nitride. This proprietary silicon nitride passivation layer provides extremely low gate leakage current and is a critical step in realizing devices with large gate width. Benzocyclobutene (BCB) deposition is done next followed by drain via BCB etching, drain pad photolithography and drain pad plating to connect the large area drain pad to the drain contact of individual devices. Finally the process is finished by thinning the wafer down to 100 um and evaporating AuGe/Ni/Au on the backside to form the source contact covering the entire bottom wafer surface.

DEVICE RESULTS

The 20A rated device has a total area of 3mm × 4.3mm. (This area includes large gate bonding pads which can be significantly reduced in size when considering designing for manufacturing). Typical output characteristics for this device are shown in Fig. 3. The maximum current measured was limited by the current source. To measure the device on-resistance, a four-point probe measurement was performed with the gate biased at 0.4V. This test shows an on-resistance of 2Ω-mm, which corresponds to a specific on-resistance of 0.26mΩ–cm^2 based on the total area of the device. Further reduction in device on-resistance can be achieved by optimization of the epitaxial structure and thinning the substrate beyond 100um.

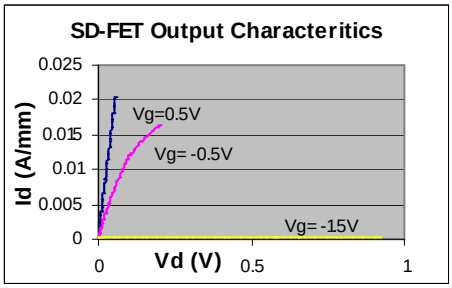

Fig. 3. Typical SD-FET output characteristics

Table 1 shows the SD-FET device parameters and compares the SD-FET to state-of-the-art Si devices with similar current and voltage ratings. As designed, the SD-FET shows high blocking voltage greater than 20V, at a gate voltage of –1V, in addition to an extremely low gate leakage current of < 0.1uA/mm as shown in Fig. 4.

TABLE 1
SD-FET DEVICE PARAMETERS COMPARED TO STATE OF THE ART SI SWITCHES

Parameter	SD-FET	Silicon	Advantage
Rsp – Specific Resistance (μΩ – cm^2)	140	350-250	• Smaller die size • Lower conduction Loss $P_{cond} = I_{rms}^2 R_{ds,on}$
Qg – Gate Charge (nC)	0.8	85	• Simplifies driving • Lower gate drive loss $P_{gate} = V_g Q_g f_s$
Vdrive – Drive Voltage (V)	~3	~10	
Coss – Output Capacitance (pF)	65	3500	• Lower capacitive loss $P_{qoss} = \frac{V_{in} Q_{oss} f_s}{2}$
Qrr – Reverse Recovery Charge (nC)	~20	40	• Lower reverse recovery loss $P_{rr} = V_{in} Q_{rr} f_s$
Turn-on / Turn off Time (nsec)	~1	10 to 70	• Lower switching loss $P_{on} = \frac{V_{in} I_{on} t_{on}}{2} f_s$ $P_{off} = \frac{V_{in} I_{off} t_{off}}{2} f_s$

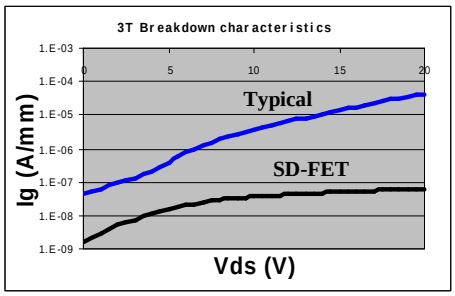

Fig. 4. Measured low gate leakage current of the SD-FET compared to that of a typical pHEMT

Turn-on and turn-off transition durations were measured to be less than 1nsec as reported in Fig. 5. This exceptionally high switching speed, unattainable by Si devices, minimizes switching losses, enabling efficient high-frequency operation essential to achieving higher power densities.

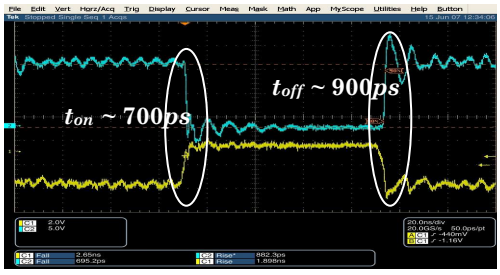

Fig. 5. Measured SD-FET turn-on and turn-off time

The measured SD-FET gate charge of 0.8nC is considerably lower than the gate charge of state-of-the-art Si devices leading to a significant reduction in the SD-FET gate driver loss. Due to higher electron mobility of GaAs, the SD-FET has a smaller die area compared to a Si FET with similar current rating. Accordingly the SD-FET output capacitance is smaller leading to lower capacitive losses. This results in the SD-FET having lower on-resistance and corresponding conduction loss than Si devices of equal size.

The low gate charge, low output capacitance and high switching speed of the SD-FET minimize the frequency-dependent switching losses, and the low device on-resistance minimizes the conduction loss. The total loss of the SD-FET is hence, lower rendering it suitable for efficient power conversion applications. The performance of the SD-FET in a multiphase buck converter topology as a drop-in replacement for a Si FET was analyzed. Plots of converter efficiency with load current for SD-FET and the Si-based implementation, shown in Fig. 6, clearly illustrate the efficiency benefit of SD-FET. Specifically, the SD-FET results in up to 9% improvement in efficiency over the Si-based solution.

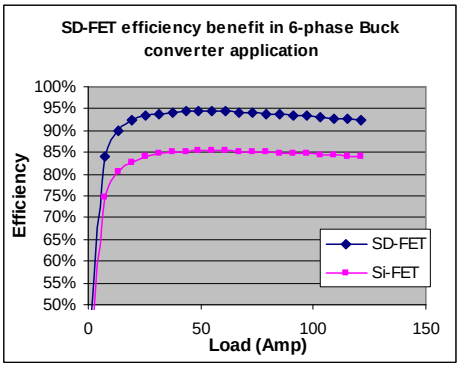

Fig. 6. Calculated SD-FET efficiency benefit in 6-phase Buck converter application

CONCLUSIONS

Achieving high power density and high efficiency to meet the challenging power requirements of next generation portable applications, demands devices capable of operating at higher frequencies. Such devices allow shrinking of the passive components, lowering of the frequency-dependent switching losses, as well as achieving faster transient response. In this paper we demonstrated the capability of the SD-FET in addressing these challenges. We also showed the compatibility of the SD-FET with large volume pHEMT manufacturing processes, making the device a cost effective power switch solution superior to Si devices in high performance power conversion applications.

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ACRONYMS

SD-FET: Substrate-Driven Field Effect Transistor
pHEMT: pseudomorphic High Electron Mobility Transistor
CMOS: Complementary Metal Oxide Semiconductor
FET: Field Effect Transistor
ICP: Inductive Coupled Plasma
RIE: Reactive Ion Etching
PECVD: Plasma Enhanced Chemical Vapor Deposition
BCB: Benzocyclobutene