Heterointegration Technologies for System in a Foil

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Abstract

This paper presents an overview of the hybrid hetero-integration approach for flexible electronic foil systems so-called "Polytronics or Smart Plastics". Core of the process is a hybrid approach based on most-polymer materials and partially-(im-)printed technologies to reach reasonable performance of systems. Moreover this approach enables the possibility to process directly on functional flexible foil substrates and to enable large area electronics.

INTRODUCTION

Multi-functional, so-called 'Smart Plastic' is considered as a second revolution after the broad industrial introduction of plastics (synthetic material) some decades ago, connecting very high innovation potential with a broad commercial relevance for a multitude of applications. At present, Polytronics summarizes development, system integration and application of active and passive electronic and photonic components, based on organic materials. The aspect of energy-autarkic systems in terms of energy storage as well as power generation and supply for flexible systems and furthermore mechanics and microfluidics is a further important aspect. A unique characteristic of polytronic systems is the potentiality of combining different functions in a single component, respectively in film based systems, consequently enabling multi-functional micro-system components in many areas of the daily life. This characteristic is considered as a future system integration platform beneath wafer-level and board-level integration. The most important objectives of polytronic systems in the upcoming years are: good value electronics, displays and solar cells; the combination of different functions in plastics and foil substrates and plastic-MEMS – towards competitive value micro-systems. Facing the challenge of large area electronics consequently requests to bring together different aspects of the broad spectrum of different favorite technologies. Systems, which distribute electronic, optical, sensor or actor functions over a large area, are used to form an interface between humans, objects and their surrounding, because they bridge the gap between the macroscopic world and the microscopic features of electronics. Today such systems are fabricated with different levels of electronic packaging, but to achieve more inexpensive products, a direct integration by coating and patterning steps on large substrates will be an appropriate and necessary way to fabricate such systems. Therefore large area electronics enables smart devices and systems at very low costs and aims at the research and development of appropriate manufacturing technologies - preferable additive processes - which will be in-line compatible and applicable to high volume production.

THE AIM OF HETEROGENEOUS SYSTEMS INTEGRATION

To strengthen this novel system integration with optimized cost-value ratio, a high scientific and technological competence must be complemented by broad multi-disciplinary and integration of various companies and institutions in the value chain, due to the very complex domain with novel materials, technologies, processes, applications and scenarios. A necessary progress in polymer electronic products is the integration of different organic materials and components in a multi-functional electronic system. Especially by integration of various technologies in 'Smart Plastic' novel applications are conceivable, so far not possible by established technologies. Technology experts unanimously predict a vast new business area. However it seems that the progress is not as fast as predicted if the last years are monitored carefully regarding promised results and announced products against published peer reviewed results and products on the market. Great potential for innovation is seen in the area of multi-functional components, OLED and polymeric solar cells in combination with energy-autarkic (mobile) flexible electronics, especially polymer electronics but also other flexible electronic technologies based on nano-filled pastes or even inorganic semiconductor materials made available on flexible substrates. The vision of smart plastic is supported by the possibility of end-user defined specifications and production at their own fabrication environment, using in-line capable and mainly additive processing of large area and low-cost systems. This means OEM foil substrates with integrated functions can be combined and customized in some final technology steps in order to serve a certain application. Polytronics facilitates for example the combination of a display with a sensor keyboard and solar cells for power management with conventional flexible silicon circuits, resulting in an efficient computer on film in a few years - to start with it - will be rather a Smart Card or a simple PDA, followed by an electronic newspaper next. Intelligent sensor surfaces are a key functionality for ambient intelligence and therefore are representative example for hetero-integration of large area systems valid for many application areas and the technology can be applied in a wide spectrum for possible products

Another application aims to a combination of electronics, sensors and actuators as well as the use of micro-fluidic and optic components in a polymeric substrate. For the first time, micro-integrated - in the future followed by even nano-

integrated - medical devices for bio-analysis and so-called personalized medicine, allow an individual therapy due to a genetic analysis and the detection of individual medical properties (bacteria, viruses, antibodies, toxins) of a patient. Complex, but cost-efficient plastic systems for bio-analysis and therapy (dosage of medicine, drug delivery) will be realized as well. On silicon basis, such lab on chip are but realized on a much higher cost level, however, the bio-compatibility of silicon technology is questionable which would not arise using bio-compatible plastics in the case of a lab on a (plastic) foil. At present, bio-analytical and nano-medical applications come to the foreground concerning applied research. Some examples are complex lab-on-chip systems for detection of viruses, bacteria and toxins, as well as the direct coupling of cells for the electrical and optical analyses of cell functions, as well as the direct and indirect signal interface (man-machine interface) to be realized in the upcoming years. Driving forces for polytronic system applications are low-cost electronics, networking as well as ubiquitous systems (ambient intelligence) and life sciences. The development time towards further application orientated polymer electronics are some estimated 3 to 5 years. Some spin-off companies want to achieve first basic applications within this year (2008). Partners for implementations come from media, paper products, printing, mechanical engineering, safety engineering and secure documents, electronics and logistics, medicine and life sciences, biotechnology, consumer electronics, toys as well as information and communication technology.

HYBRID FABRICATION PROCESSES ON FOILS SUBSTRATES

From 2001 on Fraunhofer IZM developed organic semiconductor based hybrid fabrication technologies in order to integrate successfully an in-line manufacturing process for polymer electronics enabled also for fast sheet or a roll-to-roll mass fabrication environment [1-5]. The process starts from PET-foil with a typically 200-500nm thin sputtered copper layer, which is fine-structured by photolithography and wet etching to create the source-drain-layer for the polymer electronic circuits. As switching speed of a transistor is inversely proportional to transistor length squared, metal as source and drain electrodes has been preferred because its minimum feature size is clearly below that achievable at present with polymers and printing technologies [2]. Often, metallised foils are used to create micro-structured electrical leads. A dry resist of 15 µm thickness (Dupont MX 5015) is laminated directly onto the foil substrate. Lamination takes place roll-to-roll at temperatures between 80 and 120^{o}C, UV-exposure takes place in a roll-fitted mask aligner. The exposed resist is developed moving continuously through a roll-to-roll developing unit and subsequently transferred to an etching unit. Lateral resolution is limited in photolithography by the thickness of the photo-resist. When using 15 µm thick dry resist, the yield of the patterned structures decreases considerable for feature sizes below 10 – 15 µm. Inter-digital photo-lithographically structured and wet etched Cu drain source electrodes on 50 µm polyimide foil. Cu film thickness is 500 nm, feature sizes of below 15 µm have been achieved. Work currently in progress aims to achieve large area homogeneous resist coatings in the order of 5 µm thickness by a roll-to-roll doctor-blade process in order to shrink the feature size of OFET transistors to lower than 10µm respectively. Next, the polymer semiconductor and a polymer dielectric are homogeneously coated onto the substrate via a doctor-blade process. The polymer dielectric serves as the gate dielectric of the transistors. Here, careful selection of the solvents for the different polymers plays a crucial role, as dissolution of a lower layer of polymer during coating of an upper layer from solution must be avoided. For the transistor gates two processes are evaluated at present, a screen printed process based on conducting polymer pastes and a shadow mask metal evaporation process. The gate process is followed by another screen print of the interlayer dielectric, which serves as electrical insulation between transistor and upper interconnect layer. Before this wiring plane is created by a third screen printing step, through-contacts are opened through the inter-layer dielectric, the gate dielectric and the semiconductor, to allow electrical connection of the upper interconnect/gate layer to the source-drain structures. The creation of these electrical vias is achieved by selectively cutting through this stack of polymer layers and stopping on the Cu metallization with a laser ablation process. With a spot size of 20 µm and an accuracy of 10 µm, the system shows comparable performance to stationary trim lasers. During printing of the upper metallization layer, these vias are filled with conductive silver ink and low-resistivity contacts are achieved. The figure 1 depicts a finished polymer electronic circuit, a ring oscillator, with whose help the quality of and switching speed achieved with the technology and design can be evaluated. Further circuits, like logic gates and analog circuits, are under development at present. The major target of the hetero-integration approach is the evolutionary development of hybrid technologies for large area electronics and suitable fabrication processes with a strong emphasis on production methods, equipment as well as material aspects relevant to the manufacturing processes. The polymer based hetero-integration of systems merges technologies from the rigid substrate level towards the fabrication of systems on completely flexible foils fabricated with high-volume processes. Currently a whole bunch of processing techniques is available and each of these technologies addresses different substrate bases and therefore different levels of integration. The synergy between these levels is the use of the same structuring processes, but with different performance related to specific limitations of each substrate type (e. g. resolution and registration). Immanent in the principle of hetero-integration is the evolutionary transition of these structuring methods from rigid substrate level, where currently subtractive techniques are dominating, towards flexible substrates and

additive structuring (µ-contact print, nano- and µ-imprinting or ink-jet-, screen- or even off-set printing) processes.

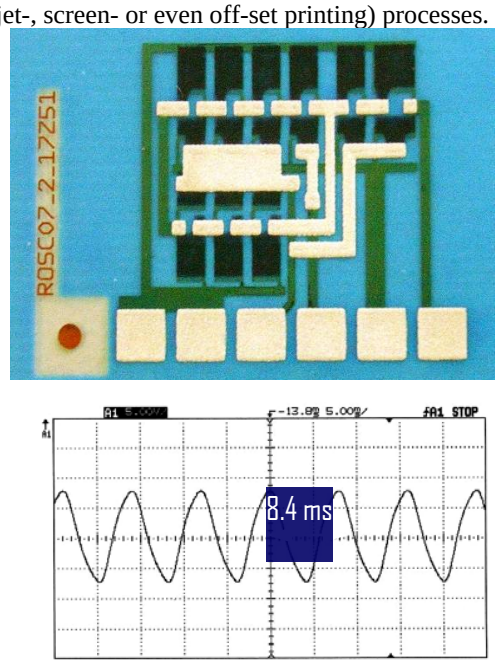

Figure 1: Completely processed ring oscillator consisting of seven inverter stages in the oscillator as well as a load inverter at the output. Transistor feature size is 15µm and oscillation frequency 119 Hz.

The technology to integrate different functional devices bases on a 2-conductor layer flex technology as depicted in figure 2, where a lithographically structured first Cu- ,metal layer is combined with a screen printed Ag-filled-polymer second interconnect layer.

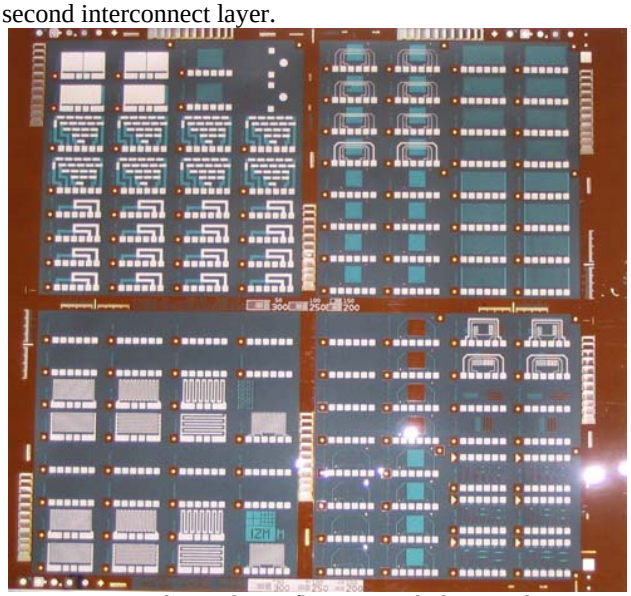

Figure 2: 2-conductor layer flex, minimal lines and spaces of lithographically structured first Cu layer: 15µm, minimal lines and spaces of screen-printed second interconnect layer with Ag-filled-polymer: 200µm, 50µm laser ablated via openings show good contact between both layers

As a compromise between functionality and cost, foil processing by means of carrier techniques plays a very important role. The development of different levels of functionality, complexity and cost for large area applications is supported by the development of suitable combination methods, e.g. selective large area structuring (SLAS) where the combination of lithography with imprint technologies leads to cost-effective large area processing technologies. Work currently in progress aims to achieve large area homogeneous additive structuring (µ-contact print, embossing, nano- and µ-imprinting) and coating processes in order to significantly shrink the feature size of OFET transistors and sensors for large area processing. In this background SLAS micro-structuring processes are developed to reach small feature sizes for devices in the range of less than 1µm in certain areas on a large area foil substrate. In the first results we still see the major problem of a µ-imprint with flexible masters, being the irregularities and defects. However they are much less pronounced compared to regular mass printing technologies (rotational, gravure offset) and the µ-imprint technologies reach a resolution of 1µm and smaller which can not be reached with any mass printing technology (rotational, gravure, offset, screen, ink-jet) at present with such a quality and edge definition.

In addition to flexible organic electronics polytronic systems can combine the assembly of thin components by related fabrication technologies on the same flexible substrates. For ultra thin chips, various assembly methods are possible like soldering and gluing processes. After performance-price considerations to apply a flip chip method with anisotropic conductive adhesives (ACA) has been selected as depicted in figure 3.

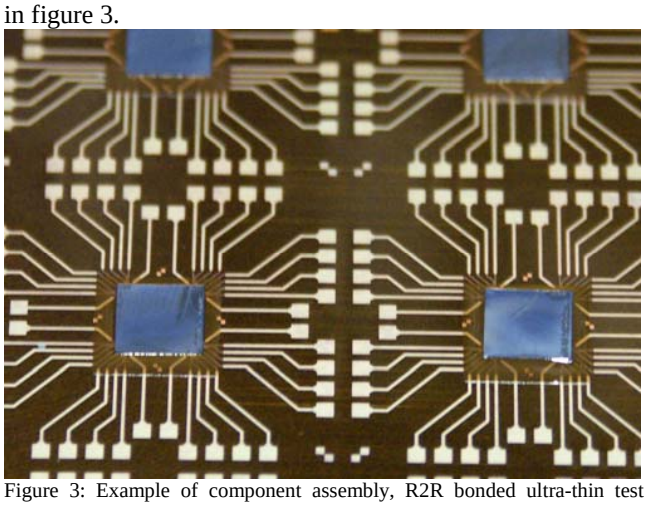

Figure 3: Example of component assembly, R2R bonded ultra-thin test chips on daisy chain test patterns on flexible PI substrates

This technique has in comparison to soldering a lower thermal stress. Therefore the shrinkage of the substrate material is minimized and the procedure is principally also suited for materials with lower thermal stability like PET. Furthermore the system height for such assembly can be kept low. The typically 20µm thin silicon chips are flexible like the foil substrate itself resulting in possible flexible high performance foil systems.

CONCLUSIONS

Polytronics will provide a cheap method for the fabrication of simple low-cost electronic, but in most cases these circuits have to be integrated in a system, which may combine different technologies (e.g. a polymer display must be integrated with pixel drivers, processor, power supply, memory I/O-circuits etc.) or different functions (e.g. thin components based electronics, printed electronics, sensors and actuators, optics and fluidics are combined for an intelligent medical bandage) leading to Smart Plastics foil systems and Plastic MEMS [4].

For flexible electronics low-cost manufacturing processes with high throughput will have to be used in future. At present it seems to be in-line industrial processes, based on the reel-to-reel (R2R) flexible substrates technique (see figure 4 or figure 2), but also fast sheet processes are considered. For low-cost OLED lighting applications roll-to-roll processes and equipment are developed intensively too.

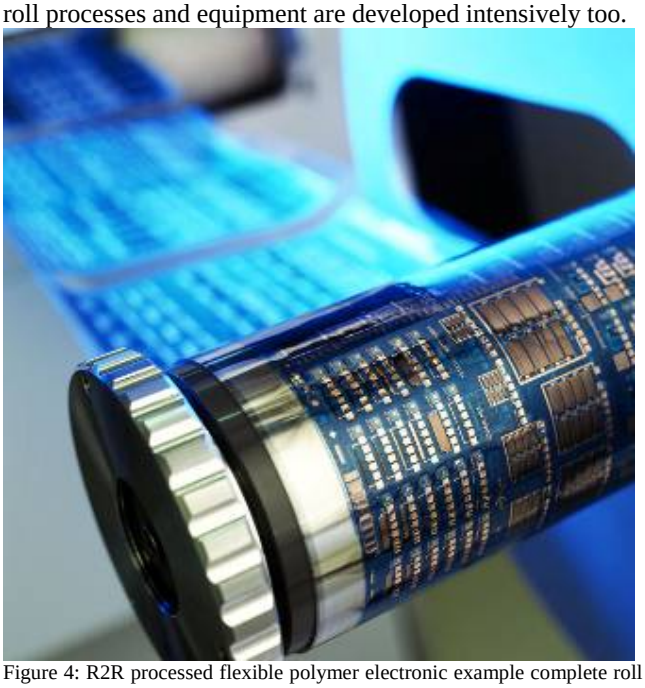

Figure 4: R2R processed flexible polymer electronic example complete roll after complete processing.

Hereby continuous flow and fast sheet are not necessarily in contradiction since the major substrate materials like plastic foils and paper are on rolls. The only difference between reel-to-reel (or roll-to-roll) and the fast sheet processes is the point of transition from roll to sheet. Some processes developments consider sheets as the solution and assume that the R2R process is not needed for large volume fabrication. But, even for a fast sheet process the substrate materials originally comes on roll and some processes can be performed more efficiently on the roll before separation to sheets. Therefore roll-to-roll enabled processing can be considered as advantage since it does not exclude the transition to sheets if necessary. The R2R process considers advantageously that the polymer electronics already starts during the fabrication process of the substrate material like the plastic foils and the paper or cardboard. In this sense it is needed to keep a roll fabrication and processing capability within the process development. At the same time R2R polytronic processing technologies can be performed on a fast sheet process too. At this time the process is yet limited in packing density and functionality, but applicable to first application demonstrators. The process performance is still somehow limited to about 12 transistors per cm² with a feature size of 15µm and about 30-50 transistors per circuit, which already allows the fabrication of arrays of analogue-digital access electronics and correspondingly large area sensor arrays. The next process integration generations are already in preparation. With a feature size of 5µm the transistor density will be increased by a factor of approximately 5 and with a feature size of 1µm by a factor of approx. 80 in relation to the present process integration based on 15µm feature size. An important condition of the process integration has always been the emphasis on cost-efficiency and therefore a direct processing on flexible foil substrates without carrier systems resulting in material costs being at present approximately 0.35€cent per cm².

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