Use of Chemical Mechanical Polishing for Planarization of GaAs Integrated Circuits

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Abstract

An interlayer dielectric process for GaAs is demonstrated in this paper. The interlayer dielectric process uses CMP for planarization of a PECVD dielectric. This paper explains GaAs CMP processing and the advantages of using a planarized PECVD interlayer dielectric.

Introduction

Chemical mechanical polishing (CMP) has been used for planarization in silicon integrated circuits for more than 20 years. To create greater device integration, it has become desirable to planarize gallium arsenide based IC's. Planarized surfaces enhance the ability to deposit thick, low loss interconnect metals. CMP has been used for digital GaAs processes in the past where increasing circuit density and reducing parasitic interconnect capacitances are of concern [1]. In contrast, for RF GaAs processes, thick metal interconnects on planar surfaces can lead to higher Q inductors, transformers, power couplers and combiners, and increase the ability to remove heat from active devices. The integration of these passive components can result in module size reduction and lower costs.

Techniques available include: spin-on glass, spin-on polymers and dielectric deposition and etch back. Each technique has draw backs: Spin-on glass needs to be cured, affecting the thermal budget of the GaAs process. Spin-on polymers can not be exposed to solvents after coating which makes further integration options limited.

CMP offers a way around the limitations of other techniques, but some obstacles must be overcome. The issues include the need for a thick layer of dielectric to completely cover tall features on the devices and adhesion of the dielectric to the substrate and the mechanical strength of the wafers.

CMP

The basic CMP process is the same for GaAs as it is for Si based IC's. The silicon process involves removing dielectric material using both chemical action and physical abrasion. Placing a wafer coated with a dielectric film in contact with an abrasive pad polishes the wafer's surface. The pad is coated with an abrasive solution. A typical abrasive solution used for silicon dioxide polishing is composed of a basic liquid that contains silica particles in suspension.

The wafers contact the abrasive surface with a defined amount of force and oscillate across the pad surface in a manner to prevent scratches and grooves made in the surface of the film. The final result is a planar surface free of scratches and with low surface roughness.

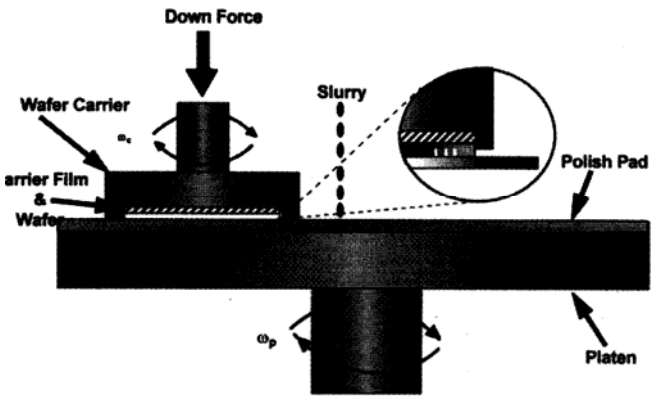

Figure 1: Diagram of typical first generation CMP tool

The process used to polish silicon oxide GaAs wafers has several important factors which effect throughput, uniformity, and process control. The process starts by loading wafers device side down onto a wafer carrier. The wafer carrier holds the wafer by vacuum on a carrier pad. The carrier pad supports the wafer during polishing and helps to minimize mechanical stress the wafer experiences during the polishing process and to improve planarity of the polished film.

Before polishing can begin, the polishing pad is prepared by pumping slurry on to the pad and is worked in to the pad with an abrasive wheel called a pad conditioner. This conditioning helps to ensure that slurry is evenly spread across the pad. The carrier then lowers the wafer to the pad surface.

The spinning pad performs the polishing. While the pad is spinning, slurry is pumped on to the pad to maintain a sufficient amount of abrasive slurry. Inadequate amount of slurry would result in poor uniformity. Too much slurry would be wasteful.

The next concern is the amount of down force needed to achieve adequate erosion rates without compromising uniformity. High down force will result in faster erosion rates but will result in poor uniformity. Figure 2 shows the polishing rate versus the down force. Another factor effecting polishing rate is temperature which is regulated by heating the pad. Temperature will effect pad lifetime, erosion rate, and uniformity.

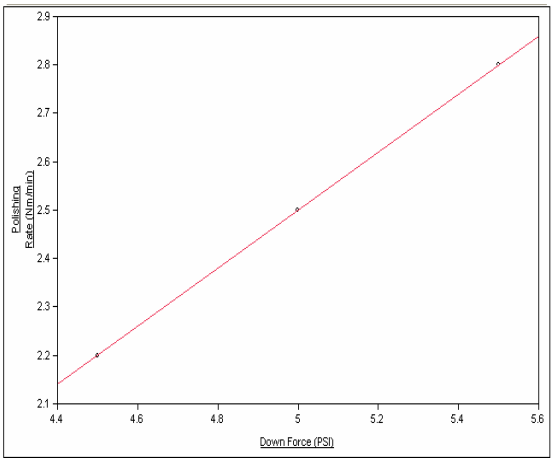

Figure 2: Down force versus erosion rate

Finally, the speed of the platen rotation, carrier rotation speed and the oscillation rate of the carrier play a critical role in both erosion rate and uniformity. Platen rotation speed and carrier rotation speed must be adjusted so that the angular speed of the platen is greater than the angular speed of the carrier. Oscillating the carrier across the polishing pad is done many times to prevent the pad from matting down in one area. The pad conditioner also works to keep the pad roughness even and the slurry well distributed [2].

In addition to the above process parameter that must be defined, the selection of slurry and polishing pads is also an important issue. The choice of slurry to be used is affected by the surface roughness target, erosion rate and ease of use. Larger particle sizes in the slurry will result in a coarse finish but a higher erosion rate. The choice of a colloidal suspension of particles in the slurry will eliminate the need for constant mixing. However, colloidal suspensions are limited in particle size. Typically, two slurries are used in one polishing operation, one for coarse polishing at high erosion rate and one for fine polishing to minimize surface roughness. Polishing pads are also selected for the effect on erosion rate and surface roughness. The choice of which polishing pads to use will be affected by whether the polishing is performed with a slurry that uses more of a chemical than a mechanical removal. Once again the typical setup is with a coarse pad for bulk removal and a fine pad for the final finish.

Another consideration is the removal of excess slurry and slurry particles from the polished wafers. Most of the excess slurry can be rinsed off the wafers using a water rinse. Water rinsing will not remove all of the slurry particles. Therefore, the final process in a CMP operation is a brush scrub.

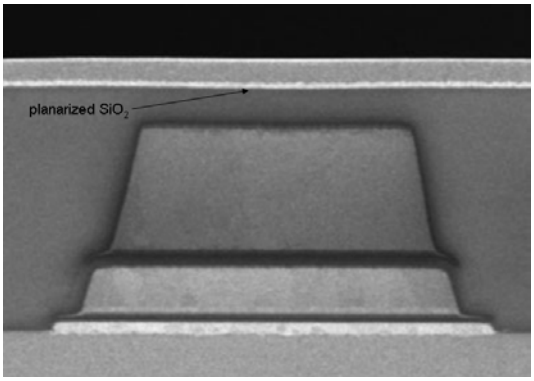

Figure 3: Planarized SiO_2 with interconnect metal stack

APPLICATIONS

The planar oxide surface as shown in Figure 3 would allow for the addition of a thick, low resistance interconnect metal on its surface. A thicker interconnect metal requires the use of thicker photo resists. If the surface is not planar, then the resist can have varying thickness across a wafer. For a given develop time, a portion of the wafer might not be totally exposed. To expose the entire wafer would require longer development times. This in turn would lower tool throughput and decrease fab wafer capacity.

A planar surface would result in uniform resist development and perhaps lower develop times.

The uses for a thick interconnect metal on a planar surface includes high quality factor (Q) inductors, transformers, power couplers and combiners, and active device heat sinks. Figure 4 shows a thick Au interconnect contacting the emitters of an HBT.

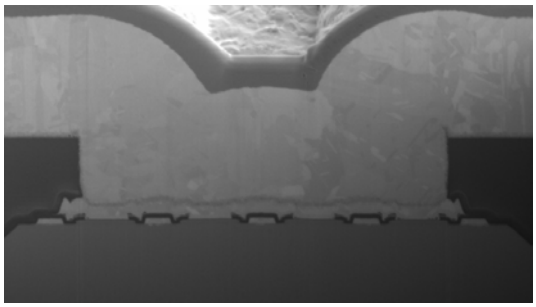

Figure 4: Thick metal HBT "heat sink"

Multiple HBTs can be connected in series by contacting the emitters to a thick Au layer. This technique would help reduce HBT thermal profiles.

An inductor using the same thick interconnect metal shown in Figure 3 is shown in Figures 5 and 6.

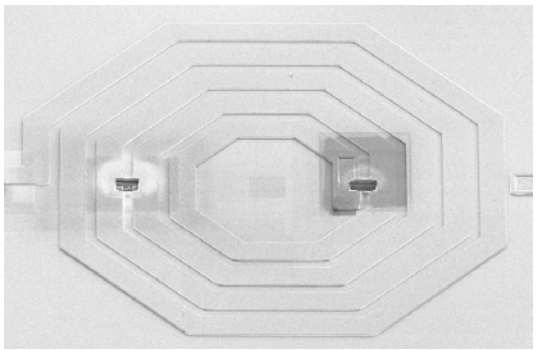

Figure 5: An inductor on the planar SiO_2 surface with FIB cuts

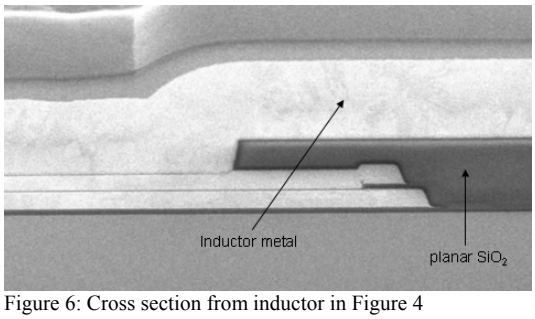

Figure 6: Cross section from inductor in Figure 4

The planar oxide surface provides the ability to scale the thickness of the metal to suit the needs of the designer. Varying the planarized low-k SiO_2 thickness under the inductor is another lever to use to vary the performance of the device. A thicker SiO_2 film would increase the inductor Q due to less loss on the bottom surface of the device [3].

CONCLUSIONS

The use of CMP SiO_2 in GaAs processes has its advantages. There are no thermal budget constraints required with SiO_2, contrary to the case of spin-on glass, nor are there any problems with exposing the planarized surface to solvents, contrary to the use of spin-on polymers.

The advantages of the planar surface include the deposition of thick interconnect metals for high Q inductors, transformers, power couplers and combiners and active device heat sinks. The planar SiO_2 process allows for the integration of more layers of interconnects if desired.

REFERENCES

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ACRONYMS

CMP: chemical mechanical polishing
Q: quality factor
PECVD: plasma enhanced chemical vapor deposition