

A uniform, reproducible and reliable GaN HEMT technology with breakdown voltages in excess of 160 V delivering more than 60% PAE at 80 V

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Abstract

We report on device performance and reliability of our 3" GaN HEMT technology. AlGaN/GaN HEMT structures are grown on semi-insulating SiC substrates by MOCVD with sheet resistance uniformities better than 3%. Device fabrication is performed using standard processing techniques involving both e-beam and stepper lithography. The process technology exhibits an excellent uniformity across a single wafer as well as high reproducibility between individual wafers of the same or a different batch. Loadpull mapping of 8x400 μm gate periphery devices with 0.5 μm gate length across all 21 cells on entire 3-inch wafers yields a PAE of (60 \pm 2)% with only 2% scatter of the mean PAE from wafer to wafer. AlGaN/GaN HEMT's demonstrate superior high-voltage stability and large efficiencies. Devices with 0.5 μm gate length exhibit two-terminal gate-drain breakdown voltages in excess of 160 V and drain currents well below 1 mA/mm when biased at 80 V drain bias under pinch-off conditions. Load-pull measurements at 2 GHz return both a linear relationship between drain bias voltage and output power as well as power added efficiencies beyond 60% up to 80 V drain bias. At 88 V an output power density of 15 W/mm with 24 dB linear gain is obtained. Reliability tests indicate a promising device stability under both radio frequency (RF) and direct current (DC) stress conditions.

INTRODUCTION

GaN electronic devices have been the subject to intense research for the past decade. Due to its wide band gap, high breakdown field, current density and saturated velocity, this material system is well suited for high temperature and high

power applications from RF to millimeter wave frequencies. AlGaN/GaN HEMTs on various substrates have raised a lot of interest for the application in future high-efficiency base station systems for next generation mobile communication, currently dominated by LDMOS technology. Using GaN technology in a transmitter, infrastructure equipment manufacturers will benefit from major improvements in system performance and flexibility. AlGaN/GaN HEMTs enable innovative circuit concepts and transceiver architecture (e.g. switch mode power amplifiers, SMPA) with high efficiency and high operating bias.

Much progress has been made in improving device performance to the extent that researchers have reported record numbers for channel charge density and power density exceeding $2 \times 10^{13} \text{ cm}^{-2}$ and 30 W/mm at 4 GHz [1].

However, several difficulties such as high voltage

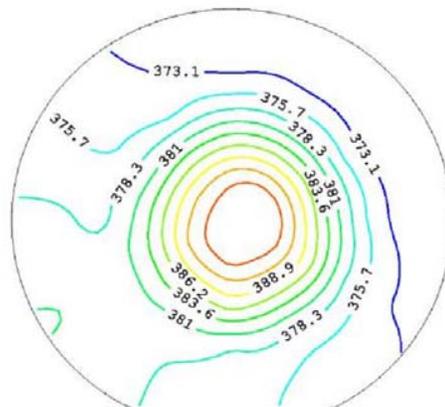


Figure 1 Sheet resistance map of a 3" AlGaN/GaN HEMT wafer.

operation stability [2], carrier trapping [3] and reliability [4] have to be overcome in order to realise the performance requirements and to fabricate devices that may be used commercially. Here, we present results from our 3" GaN HEMT technology demonstrating very promising performance and reliability data.

EXPERIMENTAL

The AlGaIn/GaN heterostructures are grown at Fraunhofer IAF by MOCVD on 3" semi-insulating 4H-SiC(0001) substrates in a modified 12x3" Aixtron 2000 reactor. Incoming substrate wafers are classified using polarized light imaging in order to examine the defect distribution. Epitaxial growth starts with an AlN nucleation layer followed by a thick GaN buffer layer and the AlGaIn/GaN barrier. For a structure having 30% Al in the barrier typical sheet carrier concentrations and mobilities are around 10^{13} cm^{-2} and $1500 \text{ cm}^2/\text{Vs}$. Contactless measurements on such structures reveal sheet resistances near $380 \Omega/\text{sq}$ that are reproducibly obtained with a uniformity better than 3% across the entire wafer, see Figure 1.

Device definition is carried out using both e-beam and stepper lithography. Device technology is based on standard III-V processing equipment and involves isolation, alloyed Ti/Al/Ni/Au ohmic contacts, field-reducing Ni/Au gates, SiN passivation, thin film resistors, Ti/Pt/Au/Pt/Ti interconnect metals and electroplated Au airbridges. The gate length of all devices discussed here is $0.5 \mu\text{m}$. Ohmic

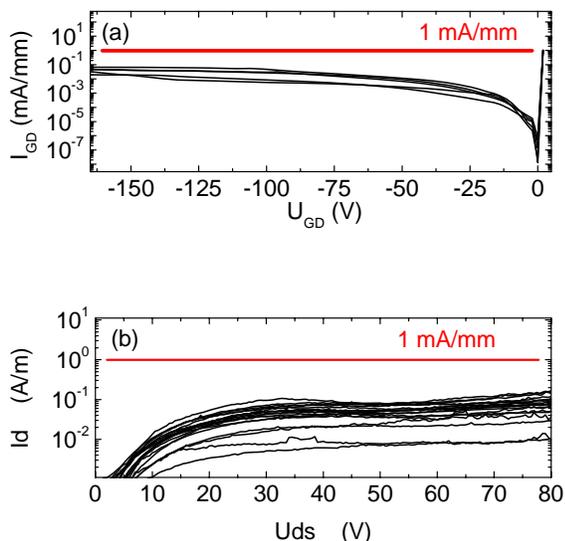


Figure 2 Breakdown characterization HEMTs with $800 \mu\text{m}$ gate periphery: (a) two-terminal gate-drain IV curves, (b) three-terminal output curve under pinch-off conditions.

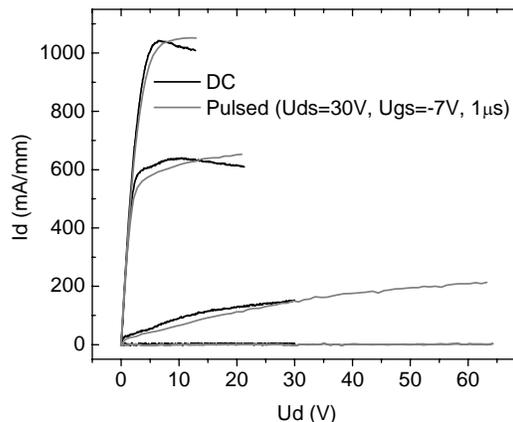


Figure 3 Pulsed and DC IV output curves of a HEMT with $100 \mu\text{m}$ gate periphery. The pulse length is $1 \mu\text{s}$ (quiescent point $U_{ds} = 30 \text{ V}$, $U_{gs} = -7 \text{ V}$) with a duty cycle of 0.1%, the gate bias is $+1 \text{ V}$, -1 V , -3 V , -5 V and -7 V .

contacts are optimized for both low contact resistance (below $0.3 \Omega \times \text{mm}$) and smooth morphology. Processed devices are examined using DC mapping, high-voltage breakdown tests, pulsed current-voltage (IV) characterization, load-pull measurements as well as DC and RF reliability tests.

RESULTS AND DISCUSSION

Results from DC mapping of fully processed wafers demonstrate the good uniformity of the process technology. For example, the transconductance exhibits a uniformity better than 3% when measured at 84 process control monitor sites distributed on a grid across the entire 3" wafer.

For efficient large signal operation, it is crucial to fabricate devices with low parasitic gate and drain currents as well as minimized carrier trapping. The high voltage stability of the devices is investigated in both two-terminal and three-terminal configuration with the breakdown voltage defined at a current density of 1 mA/mm , see Figure 2. The gate-drain breakdown voltages are better than 160 V and even at 80 V drain bias the parasitic drain currents under pinch-off conditions are well below 1 mA/mm . These results demonstrate the excellent high-voltage stability of the HEMT processed.

In order to assess dispersion (current slump) due to carrier trapping pulsed and DC IV curves are studied. Figure 3 shows output curves under both DC and pulsed ($1 \mu\text{s}$ pulse width, 0.1% duty cycle) conditions from a quiescent bias point of 30 V drain bias and -7 V gate bias. Little dispersion is visible from these curves evidencing the successful elimination of trapping effects in these devices.

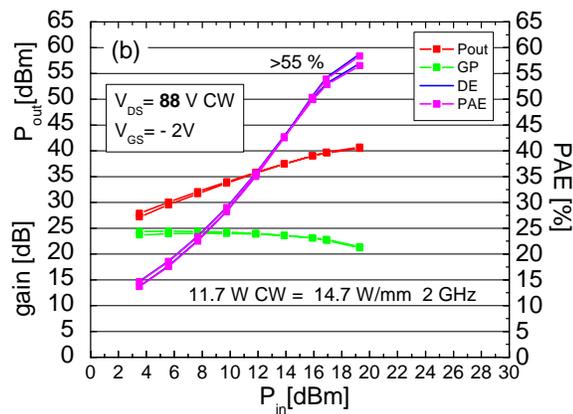
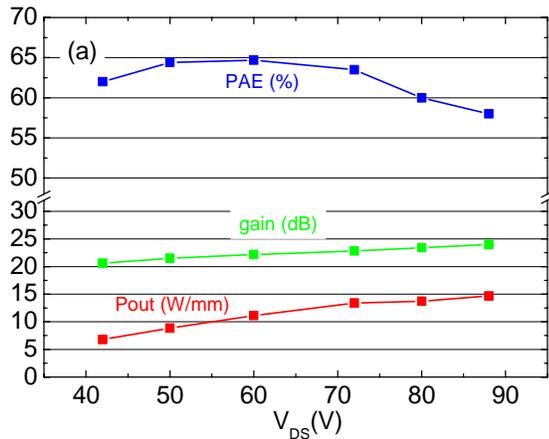


Figure 4 Loadpull measurements 0.5 μm gate length HEMTs with 800 μm gate periphery (a) versus drain bias and (b) versus P_{IN} at 88 V drain bias (two cells). Note that the PAE remains above 60% up to 80 V.

Next, the power performance of devices with 800 μm gate periphery is studied at an operating frequency of 2 GHz, see Figure 4. The dependence of power density, linear gain and PAE on drain bias up to 88 V is shown in Fig. 4(a) for a different wafer having a lower Al content in the AlGa_N barrier. The output power density scales linearly with drain bias showing the absence of knee walkout or pre-mature pinch-off at large drain bias. The PAE is beyond 60% for all bias values up to 80 V. The PAE first increases up to a drain bias of around 50 V as expected due to the reduced impact of the knee voltage on PAE but then decreases for larger bias values. This behaviour may be due to the fact that tuning is difficult for the larger impedances at large drain bias. At a drain bias of 88 V an output power density of 15 W/mm with 24 dB linear gain is obtained as shown in Fig. 4(b).

The process technology exhibits an excellent uniformity across a single wafer as well as high reproducibility between individual wafers of the same or a different batch (typically

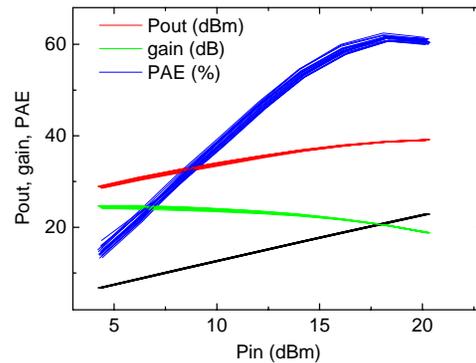


Figure 5 2 GHz loadpull mapping at 50 V of 0.5 μm gate length HEMTs with 2 \times 400 μm gate periphery across all 21 cells of an entire 3-inch wafer. Note the excellent homogeneity in output power, PAE and gain.

6 wafers). Loadpull mapping across all 21 cells on an entire 3-inch wafer (Figure 5) shows power sweeps at a drain bias of 50 V in class A/B. The maximum PAE is around 60%, the power density is near 10 W/mm and the linear gain around 25 dB. The reproducibility of epitaxy and process technology is evidenced by a low scatter in the mean PAE from wafer to wafer. Figure 6 reveals the mean PAE for all 21 cells of 12 wafers from consecutive process runs. The mean PAE is around 60% for all wafers with a scatter of just 2% for all 12 wafers.

Large periphery devices (32 mm gate width) are diced from the 3-inch wafers and mounted in industry standard ceramic packages. For these packaged chips an output power beyond 125 W is obtained on these devices with a PAE above 50% and a linear gain around 15 dB (Figure 7).

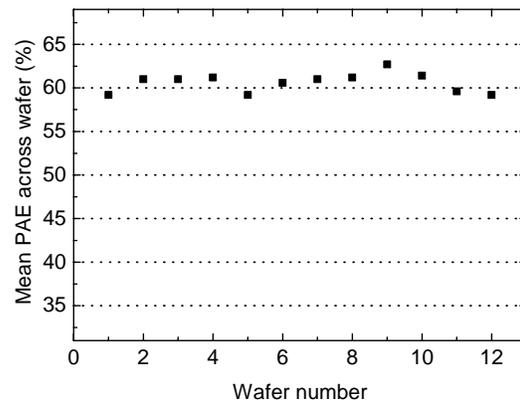


Figure 6 Power added efficiency at 50 V drain bias of 12 wafers from two consecutive processing batches.

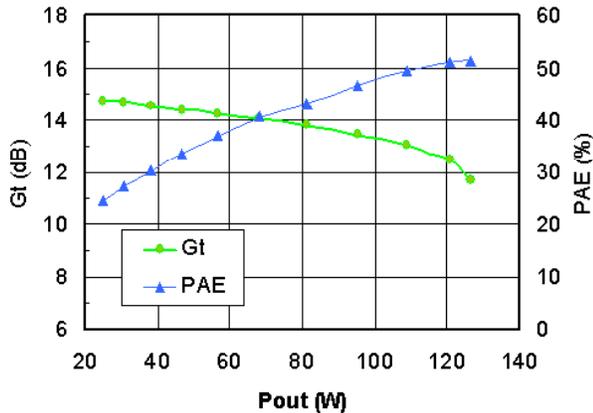


Figure 7 CW performance of a packaged 32 mm power bar at 50 V drain bias and 2 GHz operating frequency.

The one-carrier testing of the WCDMA performance is tested on power cells having a gate width of $8 \times 400 \mu\text{m}$. An ACLR at 5 MHz offset of -40 dBc is reached for an associated efficiency of $>30\%$ and the device exhibits high linearity at low average powers. Very low memory effects are observed between 100 kHz and 10 MHz where the IMD3 is independent (within $\pm 1.5 \text{ dB}$) from the tone spacing.

Reliability tests are performed first on wafer as short screening tests and then on packaged $8 \times 60 \mu\text{m}$ gate periphery devices. Both DC and RF test are carried out. The results of these tests indicate a promising device stability. Less than 10% drain-current degradation under 50 V DC-stress (50 mA/mm drain current) is observed after more than 1000 h of operation [Figure 8(a)]. Under 50 V RF stress (2 GHz, 50 mA/mm) the output power is well behaved after

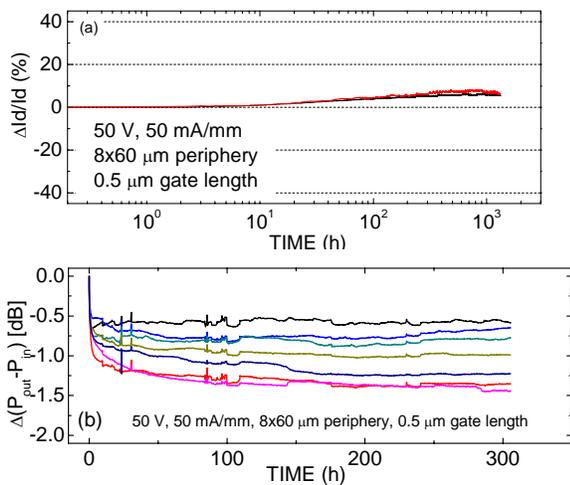


Figure 8 Reliability testing at 50 V drain bias under (a) DC and (b) 2 GHz RF conditions.

an initial drop such that it is found to be stabilized [Figure 8(b)] during the 300 h test.

SUMMARY AND CONCLUSION

High-quality AlGaIn/GaN HEMT's have been fabricated uniformly and reproducibly on 3" SiC substrates. The devices exhibit excellent high voltage stability with gate-drain breakdown voltages exceeding 160 V and parasitic drain currents at 80 V drain bias under pinch-off conditions well below 1 mA/mm. A comparison of DC and pulsed IV curves demonstrates minimized trapping behaviour leading to excellent large signal properties with PAE values at 2 GHz exceeding 60% up to 80 V drain bias. For a drain bias of 88 V an output-power-density around 15 W/mm with 24 dB linear gain and more than 55% PAE is obtained. On large periphery devices (32 mm gate width) an output power beyond 125 W is obtained on these devices with a PAE above 50% and a linear gain around 15 dB. Initial reliability test under both DC and RF conditions reveal a promising long term stability of the devices.

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ACRONYMS

- HEMT: High Electron Mobility Transistor
- MOCVD: Metal Organic Chemical Vapor Deposition
- PAE: Power Added Efficiency
- SMPA: Switch Mode Power Amplifiers
- WCDMA: Wideband Code Division Multiple Access
- ACLR: Adjacent Channel Leakage Power Ratio