Performance Improvement of High Power High Efficiency AlGaN/GaN HEMT based on the Process Design of Experiment Approach

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Abstract

Ultimately, the transistor power performance parameters depend on initial epitaxial material characteristics, device geometry and process parameters. This work presents a systematic research based on the design of experiment (DoE) approach by using minimal number of wafers. Factors of the DoE were few crucial process steps and process flow sequence. Different ohmic contacts alloying ambience, variation of surface treatment before SiN passivation and different sequence of the SiN passivation step in the process flow were evaluated. The optimal process flow was realized on 3" wafers. Pout of 6 W/mm, PAE 70% and 15dB gain at S-band for 0.2 mm device was measured at 30 V V_D that is good aligned with state-of-the art results [3].

INTRODUCTION

Remarkable progress has been made in AlGaN/GaN HEMT power and frequency performance to date achieving very high power densities and high efficiency as well as absolute power values [1-3]. However, process details and deep understanding of process parameters on device performance are seldom discussed and often are in mutual contradiction in published literature. Early deposition of SiN passivation improves current dispersion characteristics [4], while deposition of SiN after gate formation was presented with no or low current dispersion [5]. Importance of surface treatment prior SiN deposition for GaN HEMTs is hard to overestimate; variety of treatments from NH_3 plasma to NH_4OH was published elsewhere [6, 7]. All agreed in general statement, that surface modification is decisive step affecting off-state breakdown, current dispersion and resulting power and efficiency of GaN HEMT, is "a black magic" of manufacturing process.

In this work we report the systematic study of critical process parameters effect on device characteristics. Design of Experiment (DoE) methodology allows us picking out the successful sequence of process steps for required device performance; and grants a possibility to understand interplay of process steps and their physical influence. Our purpose is to improve main device performance characteristics related to the following phenomena:

- Current dispersion
- Walk-in of drain/gate current during off-state breakdown measurement
- Schottky diode non-ideality
- Two terminal and three terminal off-state breakdown

EXPERIMENTAL

Devices were fabricated on unintentionally doped $Al_{0.26}Ga_{0.74}N$/GaN layers grown by external vendor on 3" SiC wafer. To exclude wafer to wafer non-uniformity parameter from our research, and to keep cost at relatively low level, the HEMTs were manufactured on rectangular samples sawed from the same wafer. Different ohmic contacts alloying ambience, variation of surface treatment before SiN passivation and different placement of the SiN passivation module in the process flow were the factors in the DoE. Fabrication process flow is based on combination of following process modules: isolation by ion implantation, ohmic contacts with alloyed Ti/Al/Ni/Au metal stack, 100 nm SiN layer deposited as a passivation layer and the gate fabricated from Ni/Au metals. Fabrication process was finished by 6 μm of gold plating.

TABLE I GAN DOE PROCESS FLOW

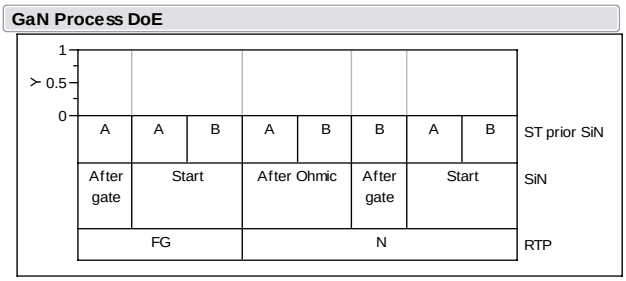

Table I presents the DoE variability chart. Forming gas (95%Ar and 5%H) and nitrogen (~100% N_2) ambient during ohmic contact annealing are labeled as "FG" and "N" respectively. SiN passivation layer at the beginning of the process is labeled as "Start", after ohmic contact alloying "After Ohmic" and after gate formation "After Gate". Two types of surface treatments, A and B, were employed prior to SiN deposition.

Total of 16 samples were run during the experiment, two samples per each sequence taken from different sites of the wafer, in order to reduce the effect of the wafer non-

uniformity. Fat FET fabrication process with the gate length of 1.5 µm and 2 µm was employed for the cycle time reduction. For the sake of process simplicity and the plenty of literature sources describing effect of the filed plate on device performance, devices were fabricated without field plate. Therefore in the DoE the target was mostly for qualitative and not quantitative results. HEMTs with 0.5 µm gate length and field-plate were fabricated on similar 3" substrate according to the best DoE results.

The rectangular samples were measured with a set of standard characterization to study the device performance. The same device with 8 µm source-drain distance, 2 µm source-gate distance and 2x100 μm^2 gate was measured across the samples. Extensive pulsed I-V and DC measurements were performed. Due to fat FET approach, S-parameters and power characteristics were measured only at the final 0.5 µm technology devices.

The DC transfer characteristics were measured at V_D = 10 V, V_G swept from -6 to +1 V, threshold voltage (V_T) was defined at drain current I_D = 1 mA/mm. Forward and reversed two-terminal Schottky diode characteristics were measured in range from -110 to +2 V. Three terminal off-state breakdown voltage was measured at closed gate, V_G = 1.5 multiplied V_T value and V_D swept from 0 to 110 V, 4 sequential measurements with 100 ms delay. V_{Boff} value was determined at where I_G = 1 mA/mm.

Pulsed I-V measurements based on AMCAD PIV system were used to evaluate the device performance. Pulse width is 450 ns, with duty cycle 10%. The pulsed IV data are measured similar to [8], with extension of IV curves from two to four quiescent points and two V_G steps, $V_G = V_T$ and V_G = +1V, further referred as I_{MAX} curve. The schematic view of pulsed IV with quiescent points is presented in figure 1.

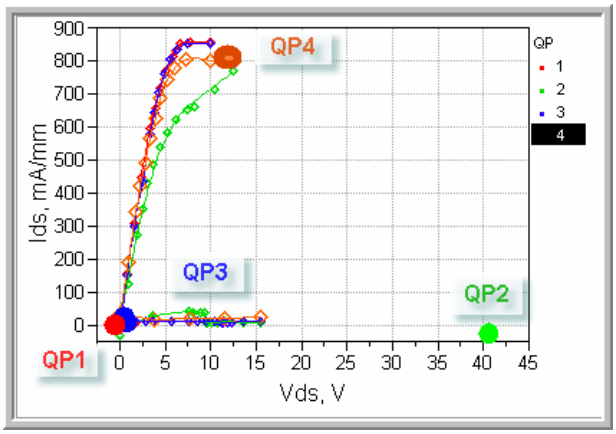

Figure 1 Schematic view of pulsed IV curve with outlined quiescent points.

The following designations are used further in the text: QP1 stands for [0; 0] of [V_G; V_D], QP2 for [-6; 40], QP3 for [-6; 0] and QP4 for [+1; 6]. QP3 and QP4 points help to understand the origin of the current dispersion and separate surface and bulk relative contribution into the current dispersion effect. I_{DMAX} is defined as drain current at V_G = +1; V_D = 8V, I_{GMAX} is defined as gate current at V_G = +1; V_D = 8V.

From these curves we defined six figures of merit for drain and gate current changes as a result of current dispersion. In general form we can refer as CCId_***i*** as ratio of I_{DMAX} measured from QP***i*** to I_{DMAX} measured from QP***1*** and multiplied by 100 (for %). For gate current consequently CCIg_***i*** defined as ratio of I_{GMAX} measured from QP***i*** to I_{GMAX} measured from QP***1*** and multiplied by 100, where ***i*** changes from 2 to 4.

Results & Discussion

Analysis of the data reveals few interesting results. We will start from the current dispersion effect. CCId_2 relates to both drain and gate lag with high electric field between gate and drain, resulting in the presence of hot electrons. The hot electrons can arise from buffer/channel region or as a result of a tunneling from the gate edge. They could be trapped into existing traps or create an additional defects/traps both in semiconductor/SiN interface and in semiconductor itself.

At the same time, CCId_3 and CCId_4 are varied between 80% and 90% and have only minor dependence on process parameters and process sequence. From physical point of view, CCId_3 relates to gate lag only, with a presence of low electrical field; *i.e.* to an interface between metal and semiconductor and region in the gate vicinity. CCId_4 relates to situation when the HEMT is fully open, and all possible electrons flow in the 2DEG channel and penetrate into nearby GaN and AlGaN layers. Electron trapping can occur only in bulk/channel interface region.

Comparison of CCId_2, CCId_3 and CCId_4 for all experiments shows that CCId_2 has the highest current dispersion value with range between 15% and 90%, depending on the experiment.

Summarize these results and having in mind that all devices were fabricated on the same wafer, we can conclude that surface is the main factor affecting current dispersion phenomena.

Figure 2 shows at a glance results for CCId_2 as a function of the process flow and the applied treatments. It seems that the best process sequence is a combination of an alloying in N_2 ambience, SiN deposition after ohmic contacts and type B surface treatment.

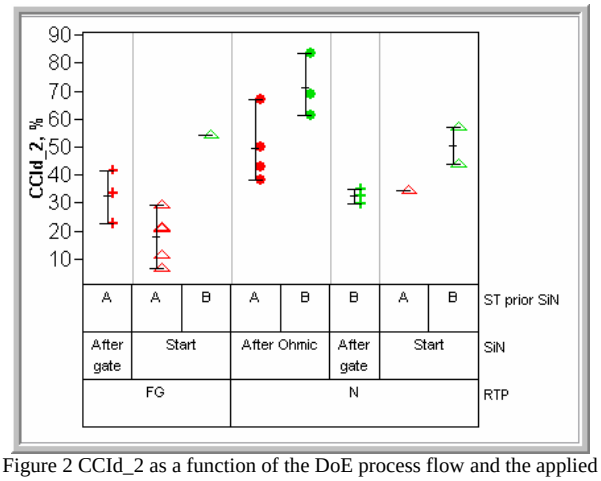

Figure 2 CCId_2 as a function of the DoE process flow and the applied treatments.

Due to the fact that not all of the process flows and treatments combinations were evaluated, each parameter has to be evaluated independently for the best result. By selection on the relevant experiments from the DoE, comparison between each process flow and treatment we can evaluate if there is any other combination that may give better results. Figures 3, 4 and 5 present surface related drain current dispersion as function of the RTP ambiance, SiN passivation placement and the surface treatment respectively.

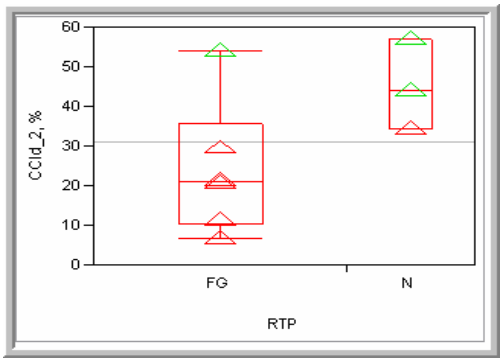

Figure 3 CCId_2 as function of the RTP ambiance.

Analyzing each plot we can conclude that modules with N_2 ambience, SiN deposition after ohmic contacts and type B surface treatment are superior comparing to other process combinations.

This is quite surprising result, because from the first principles the SiN deposition from the process "Start" is expected to be the best case [4]. Addition the absolute values of I_{DMAX} to analysis will complete the picture: the highest absolute value measured from QP_1 is for SiN start, I_{DMAX} = 1150 mA/mm, but only when combined with surface treatment B. When combined with the surface treatment A I_{DMAX} is in the range of 800÷850 mA/mm. I_{DMAX} values measured from the quiescent point QP_2 are 570 mA/mm and 120 mA/mm respectively. This proves the crucial importance of the surface treatment.

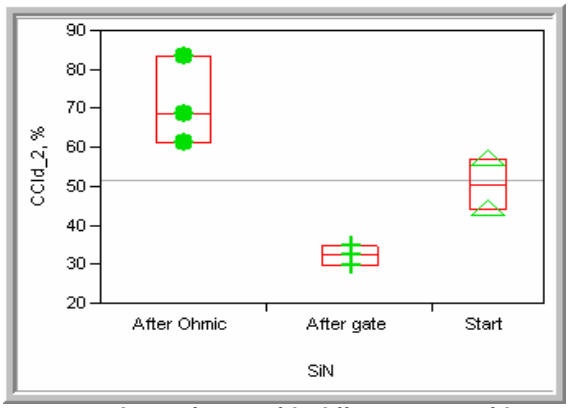

Figure 4 CCId_2 as a function of the different sequence of the SiN passivation step in the process flow

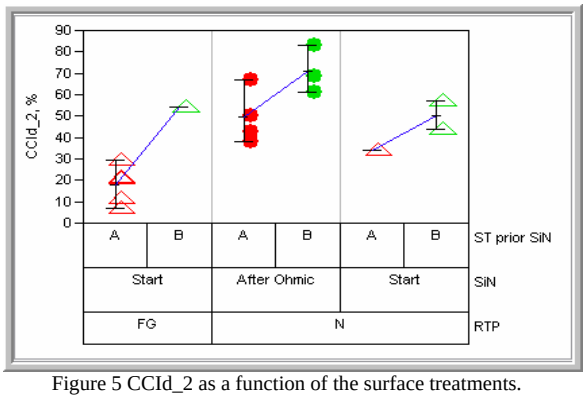

Figure 5 CCId_2 as a function of the surface treatments.

DoE approach permits to construct empirical models to evaluate interplay of various sets of measured parameters. Thorough examination shows that the strong correlation exists between surface related drain current dispersion and measured gate parameters: I_{GMAX} and CCIg_2.

The higher the absolute value of gate current I_{GMAX}, the higher current dispersion exhibits device under test. And the higher change of the gate current CCIg_2, the higher current dispersion exhibits device under test. It is interesting to note that the change of the gate current value is positive, i.e. when current dispersion is exist, the gate current leakage value increases. Figure 6 a) and b) shows the modeled values of CCId_2 as a function of the gate current absolute value and the change of the gate current. Because of non-relevant layout of the fat FETs, one should not look for quantitative but only for qualitative models. This behavior can be explained if we suppose that the current dispersion is proportional to surface states concentration. High density of surface states concentration may results in high gate leakage through hopping, possible Frenkel-Pool conduction mechanism. At the same time, high surface states density lead to high level of current dispersion, as was shown in [9].

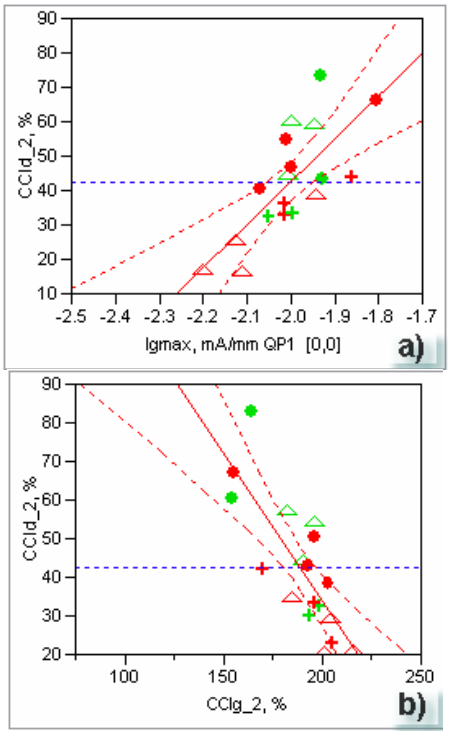

Figure 6 Constructed empirical model related CCId_2 to I_{GMAX} (a) and CCId_2 to CCIg_2 (b).

This hypothesis explains dependence between power added efficiency (PAE) and gate leakage values, presented in [8]. The higher observed gate leakage, the higher current dispersion, results in lower output power and the lower PAE could be observed.

We have also found that the ideality factor of Schottky gate diode is correlative to the drain current dispersion. Ideality factor has negative correlation with CCId_2 value. This confirms our hypothesis about the surface states.

The best process flow was realized on 3" wafers. P_{OUT} of 6W/mm, PAE 70% and 15dB gain at S-band for 0.2 mm device was measured at 30 V V_D. Figure 7 presents the measured power performance.

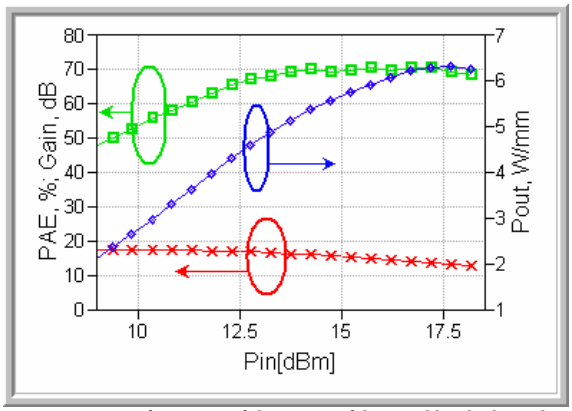

Figure 7 Power performance of the HEMT fabricated by the best chosen sequence.

CONCLUSIONS

Thorough investigation of process impact on device performance was done. DoE methodology proves itself as a powerful tool for fast process development and physical insight. Best process sequence with superior device performance was achieved.

Strong correlation between drain current dispersion and gate leakage, as well as Schottky ideality factor was revealed in this work. The physical explanation, based on access concentration of surface states, is in good agreement with published previous results of other groups. P_{OUT} of 6 W/mm, PAE 70% and 15dB gain at S-band for 0.2 mm device was measured at 30 V V_D that is good aligned with the state-of-the art results [3].

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ACRONYMS

HEMT: High Electron Mobility Transistor
DoE: Design of Experiment
RTP: Rapid Thermal Process
PAE: Power Added Efficiency