

Via etching in BCB for HBT technology

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ABSTRACT

The high integration level associated with HBT- GaAs devices especially ones consisting of analog and digital components typically requires an additional interconnection level in order to achieve a planarization of the transistor mesa topologies. This inter-metallic layer avoids cracks in metals in upper metallization levels at high topography. In this study we developed and characterized the via patterning of BCB (Benzocyclobutan) as an inter metallic layer for GaAs HBT applications. For such an interconnection system a high selectivity to the etch stop layers is required for the high aspect ratio vias. In addition the BCB thicknesses are different due to the planarization. This work shows the capability of via etching with an aspect ratio up to 2 in the BCB interconnection levels using a silicone oxide hard mask. The dry etch is performed in an ICP etcher using fluorine (SF₆, CHF₃, CF₄) and oxygen chemistry. The dry etching consists of three etch steps. At the first step the silicone oxide is etched using a resist mask. Secondly the BCB is structured and at the third step the remaining silicone oxide is removed. After etching no resist removal is necessary and in addition the BCB surface is deoxidised by fluorine plasma.

INDRODUCTION

BCB is compatible with low cost solutions for the process integration of inter- metallic dielectric or passivation layers. BCB is spun on the wafer using state of the art resist coaters. The BCB itself is delivered as pre polymerised product (40-60%) that is coated on the wafer. After spinning, the BCB is polymerised in a curing oven. The BCB is linked up to 75 –100 % in a cross linked 3D structure as depicted in Figure1.

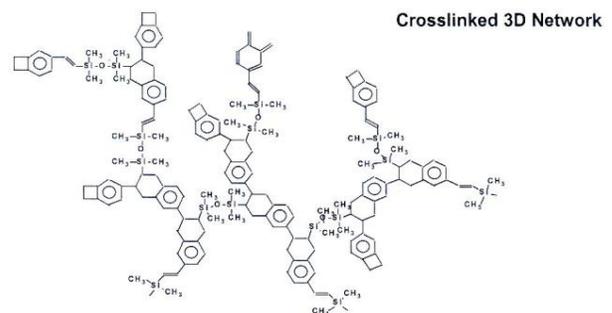


Figure1: Chemical structure of cured BCB

The crosslinked BCB is then etched by a fluorine/oxygen plasma. The fluorine chemistry binds the silicon in the cross linked polymer and the oxygen oxidizes the polymers which build up volatile etch products.

In this work the BCB is used as an inter-metallic layer. In order to achieve a good step coverage of the metallisation inside the via hole, the

taper angle of the via has to be perpendicular or positive. The critical dimension of the vias is 2 μm for this application.

RESIST VS SILICON OXIDE ETCH MASK

In general a resist mask would be the first choice as it offers advantages in terms of cost for BCB dry etching. From a technical point of view there exist arguments against the use of a resist mask for via etching in BCB at CD of 2 μm. The CD loss is very high that is caused by poor sidewall polymerisation using a resist mask. As the etch selectivity of BCB to resist is about 1 the resist thickness has to be very high. In this case we use a 6 μm resist thickness (definition of resist thickness explained later). Additionally there arises negative effects at openings when the aspect ratio (AR) is equal or greater than 0.75. These effects are etch lag in small vias caused by reduced via bottom and increased via sidewall reactions during dry chemical etch. This increase in sidewall reaction lead to a bowed via hole profile that depends on the taper angle of the resist profile. The resist profile is adjusted by the focus value of the lens to the top of the resist surface at the exposure process. Positive defocus value means point of focus plus greater distance from the lens to the resist surface and negative values vice versa. Figure 2 shows SEM cross sections of 4 μm vias with a variation of defocus values. As the etch selectivity is 1, the resist profile is transferred into the BCB. Furthermore it can be seen that a perpendicular profile shows a strong bowed and negative tapered profile in the BCB.

Further characterisation of the etch depth of 4 μm via (AR about 0.75) compared to the openings at the 70 μm (AR about 0.05) wide structure of the saw line shows that the etch depth depends on the defocus value. That means if the resist profile becomes perpendicular (defocus value 0 μm) at AR of about 0.75 there exists an etch lag that causes a reduced etch depth of about 20% (Figure3) compared to the 70 μm openings. Further results show that with increasing AR, the etch lag increases.

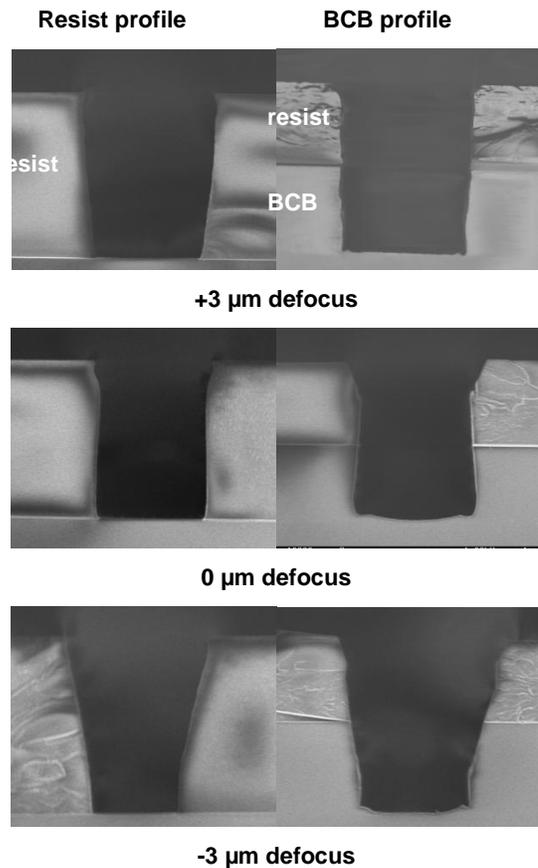


Figure 2: resist and BCB profile depending on defocus value of exposure process

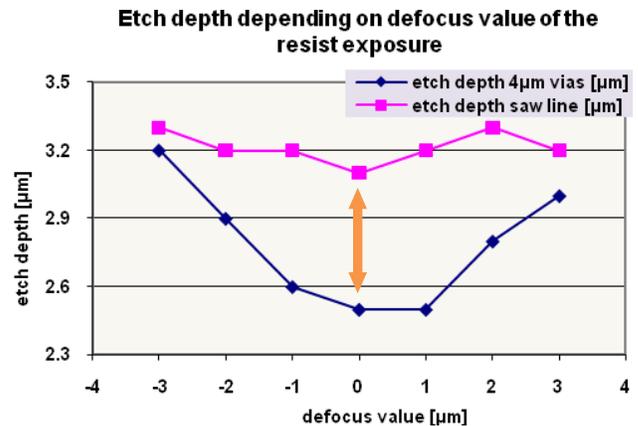


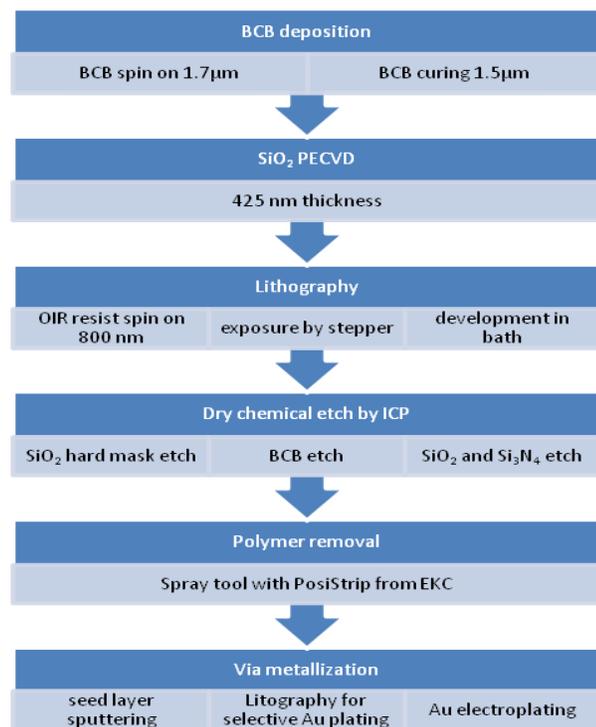
Figure 3: etch depth depending on defocus value or slope angle of the resist opening

The CD loss ($CD_{etch} - CD_{resist}$) of about 1.0 μm after etch on via bottom does not depend on the

resist profile. Of course, it is depending on the dry etch process parameters and the sidewall polymerisation that is influenced by the type of etch mask used (see characterisation etch process later on). In case of an oxide hard mask the CD loss is about 0.4 μm . In both cases a high CD loss exists when compared to a 2 μm via. The difference is that the lithography of a 2 μm via in a 6 μm thick resist is difficult. In order to compensate the CD loss of 1.0 μm the CD in the resist has to be 1.0 μm (in case of a 2 μm via) in a 6 μm thick resist. Compared to the oxide hard mask process it is easy to compensate a CD loss of 0.4 to 1.0 μm when necessary. The oxide is structured by an 800 nm thick resist mask by dry chemical etching. Furthermore the oxide hard mask process shows no bowed via profiles, no etch lag and the taper angle of the vias do not depend so strongly on the mask profile. These points lead to the motivation of the integration of the oxide hard mask process.

PROCESS FLOW

The process of realising the interconnection level using a hard mask process consists of six process steps. The flow chart below shows the process steps in detail:



The BCB shrink about 10% during curing compared to the thickness after coating.

The following sections discuss the effects of focus on the BCB topography, the dry etch process and the polymer removal. Finally results of the electrical contact resistance of metal 1 and 2 will be presented.

BCB TOPOGRAPHY

The BCB thickness after curing on a blanket wafer for this process is 1.5 μm . The HBT structures are about 3 μm at this level measured from the bottom up to the first metal layer above the emitter mesa. The height of the surface differs 1.2 μm measured from top of the BCB at the saw line to the top of the BCB near by the emitter contact. The step size reduces to 300 nm if there is 3.0 μm BCB coated and at 4.5 μm BCB coating the step size reduces to 200 nm. That means the most effective planarization is reached using a BCB thickness between 3.0 to 4.5 μm . The poor planarization is not important for the device itself, but as side effect the parasitic capacitances are increasing between metal lines. However, reduced planarization impacts the process integration at the following lithography step.

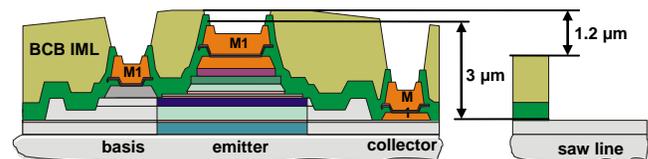


Figure 4: Schematic of the HBT transistor after the BCB via etch

Measurements show that the resist thickness is about 60% of the coated resist thickness at the emitter contact using 1.5 μm BCB. For 3 μm BCB coated wafers the resist coverage at the emitter contact is about 85%. This poor planarization of the BCB coating defines the target for the resist thickness.

The BCB thickness varies from 0.4 μm (emitter contact) to 3.0 μm (collector contact). The BCB thickness at vias in the digital part is about 1.5 μm with a critical dimension of 2 μm .

DRY ETCH PROCESS AND POLYMER REMOVAL

The dry etch process is undertaken using an ICP System OMEGA supplied by Aviza. The tool works with two RF generators. One generator powers the coil around the chamber and the other supplies the wafer chuck with RF power. The etch process consists of 3 steps (see figure 5) with different fluorine gases, oxygen and argon.

Steps:	1 SiO ₂ etch	2 BCB etch	3 SiO ₂ /Si ₃ N ₄ etch
CF ₄ [sccm]	10	-	25
CHF ₃ [sccm]	25	-	10
Ar [sccm]	15	-	15
O ₂ [sccm]	-	30	-
SF ₆ [sccm]	-	5	-
pressure [mtorr]	10	5	10

Figure 5: process steps and gases of dry etch process

Etch rate and selectivity of silicon oxide to resist depend on the ratio of the CHF₃ to CF₄ flow. By increasing the ratio of CHF₃ to CF₄ the resist etch rate decreases and the SiO₂ etch rate remains constant. For the first step the selectivity of SiO₂ to resist in our case is 1.3 that shows good results for the hard mask opening.

At the second step the BCB etch demands a high selectivity of BCB to silicon oxide. As higher the selectivity as thinner the oxide hard mask can be used for structuring the BCB. The SiO₂ etch rate depends on the fluorine content in the plasma. Above there is mentioned that the Si in the BCB is bind by fluorine chemistry. But there is just needed few fluorine to react with the silicon in the BCB. The remaining hydrocarbons are mainly etched by atomic oxygen. As O₂ is highly electro negative and due to its radical behaviour it is able to abstract very effectively hydrogen atoms out of hydrocarbons which generate radicals of hydrocarbons. These new radicals cause a mechanism of radicals generation and react to volatile low level molecules like CO, CO₂ and H₂O. By reducing the SF₆ flow from 10 to 5 sccm the selectivity of BCB to SiO₂ increases from 5 to 9. Figure 6 shows an opening at the saw line and at a 4 μm opening with the remaining hard mask of 50 nm on top of the BCB after both steps.

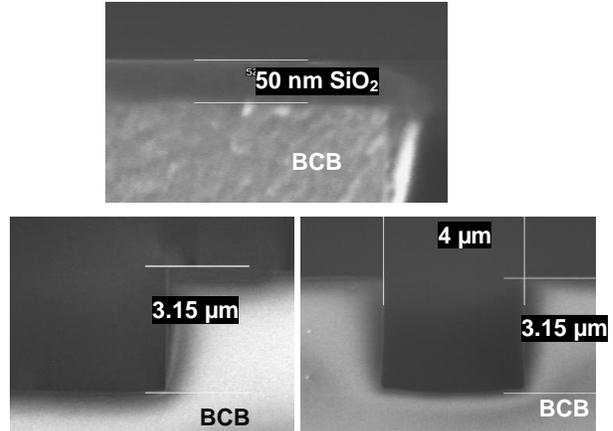
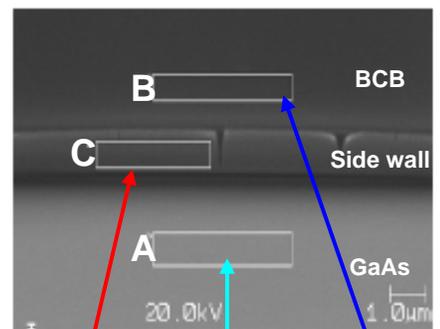
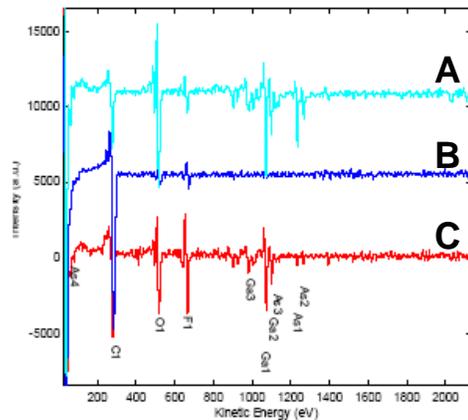


Figure 6: BCB etch depth and profiles after dry etch step 1 and 2

At the third step the SiO₂ hard mask and the Si₃N₄ inside the via is etched.

The high anisotropy of this etch process is achieved by an active side wall passivation that is built up during etching. This sidewall passivation consists of compounds of metallic fluorides and oxides. Furthermore the BCB surface after the third etch step shows nearly no oxide and fluorine elements in the Auger spectra (Figure 7).



Side wall saw line, bottom saw line, BCB surface

Figure 7: Auger spectra after the dry etch process

That shows that the BCB is not oxidized and there exists no risk of cracks in the BCB. The side wall polymerisation is removed in a spray tool using a polymer remover. Figure 8 show a clean sidewall after solving in the remover.

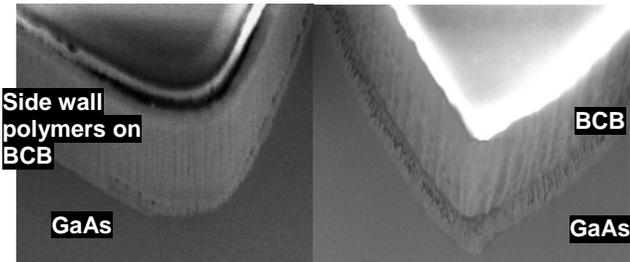


Figure 8: BCB side wall before(a) and after (b) polymer remover

This side wall passivation enables a high anisotropic etch of vias with an aspect ratio up to 2 as shown in this work (Figure 9).

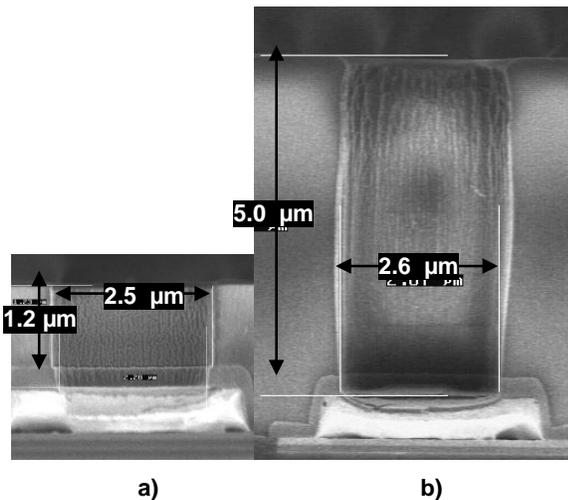


Figure 9: Via in BCB with aspect ratio 0.5 (a) and 2 (b)

INTERCONNECT ON DEVICE

The process module has been electrically characterized on a contact chain in a PCM module by measurements of the electrical contact resistance. Two 4 inch wafers have been measured, with 20

PCMs with two different contact chain lengths, being measured. Two contact chains of 288 and 1344 contacts of the Metall 1 to the Metall 2 layer separated by the BCB intermetallic layer. The CD of the via holes is 2 μm. As shown in the chart below, the average and range of the resistance rises when increasing the BCB thickness spun on the wafer. This effect can be reduced by improving the metallization process for high aspect ratio interconnects.

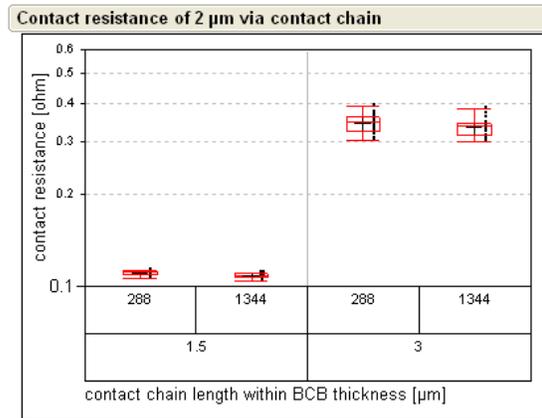


Figure 10: via contact resistance

CONCLUSION

This work has shown, it is possible to integrate an cost effective BCB interconnect level by covering topographic steps of up to 3.0 μm with BCB thicknesses of up to 4.5 μm which can be structured by an oxide hardmask process with aspect ratios of 2 with a CD of 2 μm. Additionally one lithography level can be avoided for the Si₃N₄ opening before the BCB deposition compared to the process module using a resist mask for BCB via etching.

ACRONYMS

- HBT: Heterojunction Bipolar Transistor
- ICP: Inductive Coupled Plasma
- CD: Critical Dimension

