Advanced multilayer interconnect technology for switch ICs using InP HEMTs

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Abstract

An advanced four-level interconnect technology has been developed to make high-impedance ITLs with a low crosstalk in compact switch ICs using InP HEMTs. The interconnect consists of a 2-μm-thick 3rd Au metal layer, 5-μm-thick 4th Au metal layer, and 5-μm-thick BCB insulator layers in addition to the ordinary 1st and 2nd metal layers. This technology has three key features: RIE using O_2/CF_4 gas to form via-holes with aspect ratio of over 1 in thick BCB film; selective electroplating with low current density to form thick Au layers with good thickness uniformity; and a pad stack structure with a via-contact array to improve the bonding reliability. Measured RF characteristics of TFMS lines indicate the usefulness of this technology in compact switch ICs.

INTRODUCTION

A wideband switch with multiple input/output ports is a key device for wired and wireless broadband networks and measurement systems. One of the most promising ways to achieve such a switch is to utilize InP HEMTs, which have a low product of on-resistance and off-capacitance [1], in a compact configuration. We have demonstrated a 4x4 switch matrix using InP HEMTs with a two-level interconnect [2]. However, in the compact configuration, further increasing port count while maintaining wideband performance would be difficult as long as an ordinary two-level interconnect is used because it only allows one to utilize coplanar waveguides as ITLs.

In this paper, we present an advanced four-level interconnect technology for compact switch ICs with large-port-count using InP HEMTs. Multilayer interconnect lines allow us to utilize densely arranged low-loss microstrip lines with high characteristic impedance as the ITLs.

STRUCTURE

Figure 1 shows the four-level interconnect structure fabricated by this technology. The interconnect consists of a 2-μm-thick 3rd Au metal layer, 5-μm-thick 4th Au metal layer, and 5-μm-thick BCB insulator layers in addition to the ordinary two-level interconnect, which consists of a 0.6-μm-thick 1st Au metal layer, 2-μm-thick 2nd Au metal layer, and 1.6-μm-thick BCB insulator layer. Electroplating is used to form the 2nd, 3rd, and 4th Au metal layers. Electroplated Au is very suitable as a metal layer because of its low resistivity and ease of processing to form a thick film. BCB is very suitable as an insulator film because of its low dielectric constant (2.6), ease of processing to form a thick film, and its low cure temperature (250°C or lower), which is very important for eliminating thermal damage to InP HEMTs.

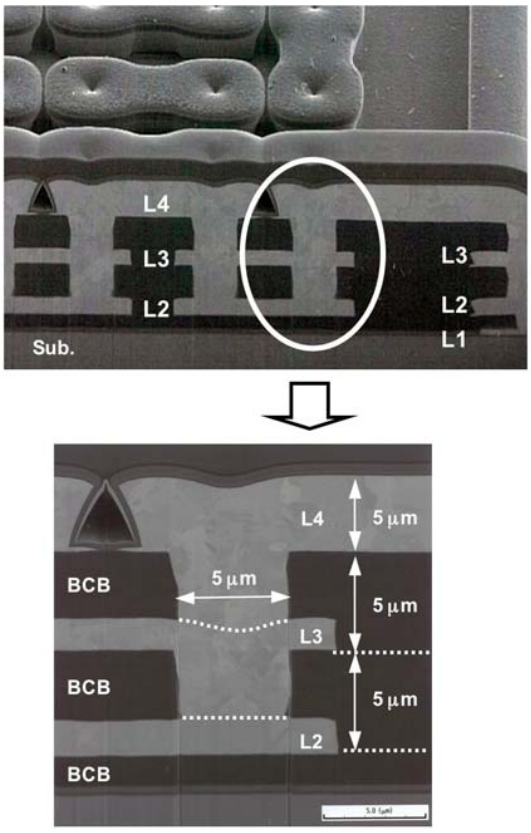

Fig. 1. Cross-sectional microphotograph of the four-level interconnect structure.

EXPERIMENTAL

Figure 2 shows the main steps of the fabrication process. An insulator film of 5-μm-thick BCB is spin-coated on a 3-inch wafer with the lower metal layer and cured at 210 ˚C for 40 min. Via-holes are formed in the BCB layer by RIE using O_2/CF_4 gases and a photoresist mask [Fig. 2(a)]. After etching, the photoresist mask is removed by wet etching. Then, thin layers of adhesion metal (W) and seed metal (Au) are continuously deposited by sputtering [Fig. 2(b)]. Thick Au layers are formed by selective electroplating with photoresist mask [Fig. 2(c)]. After electroplating, the photoresist mask is removed by wet etching. Then, unnecessary thin layers of adhesion metal and seed metal are removed by ion milling with plated Au as mask. Finally, the residue of metal atoms on the insulator film is removed completely by RIE using SF_6 gas [3] [Fig. 2(d)]. The whole process is repeated after finishing the top-level metal layer fabrication. Finally, the wafer is cured at 250 ˚C for 60 min for full polymerization of BCB.

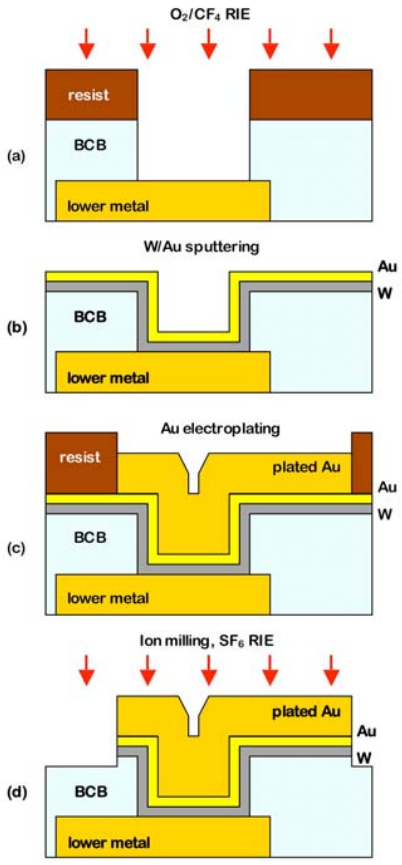

Fig. 2. Main steps of the fabrication process.

This technology has three key features: RIE using O_2/CF_4 gas to form via-holes with an aspect ratio of over 1 in thick BCB film; selective electroplating with low current density to form thick Au layers with good thickness uniformity; and a pad stack structure with a via-contact array to improve the bonding reliability.

Via-holes were formed in thick BCB film by RIE with a photoresist mask using O_2/CF_4 gas. Used gas mixture was 1:1 O_2/CF_4 because the maximum etch rate was achieved with this gas mixture. The problem is etching residue on the sidewall of the holes. This residue depends on the pressure during RIE and decreases with increasing pressure. However, RIE at high pressure causes large side etching of holes. To overcome this problem, we employed RIE with a high pressure of 5 Pa and formed via-holes by repeating the etching process (photolithography, etching, photoresist removal). As a result, we were able to form holes with the minimum diameter of 4 μm in BCB film with a thickness of 5 μm, as shown in Fig. 3.

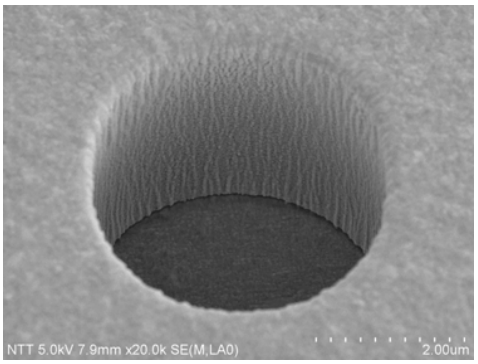

Fig. 3. SEM image of a via-hole with a diameter of 4 μm, which is coated with a thin metal layer.

Thick Au layers were formed by selective electroplating with thick photoresist mask and by ion milling, as shown in Fig. 4. The problem in the selective electroplating is a micro loading effect in the thickness of the plated Au layer. In the area of dense patterns, the plated Au in the center of the area is thinner than that on the perimeter. This effect depends on the current density for plating. Figure 5 shows the current density dependence of thickness variance and process time. The thickness of plated Au is about 5 μm. The thickness variance decreases with decreasing current density. However, low current density increases process time. As a compromise, we employed a current density of 5 mA/cm^2 and obtained thickness variance of 5.6% in 5-μm-thick Au layer.

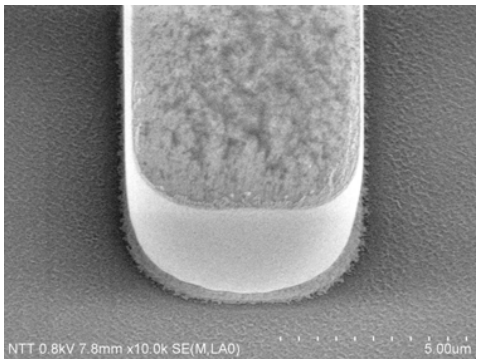

Fig. 4. SEM image of the 4th Au metal layer with 5-μm thickness and 6-μm width, formed by electroplating.

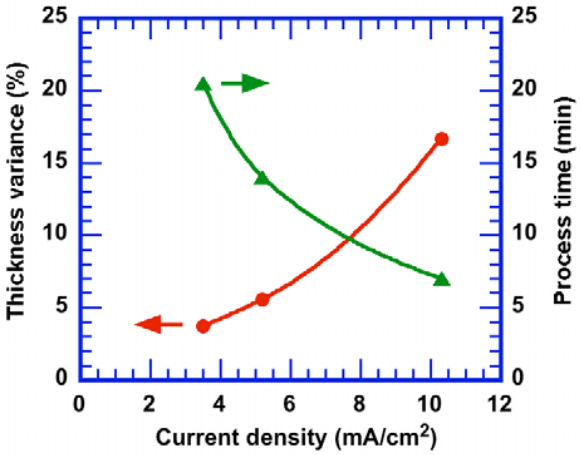

Fig. 5. Dependence of thickness variance and process time on current density for plated Au with 5-μm thickness.

In wire bond IC products, bond-pad peeling and bond-wire breaking have been recognized as two dominant weaknesses. The reliability of a bond pad depends on its structure. We investigated two kinds of pad structures: a pad stack structure without BCB film between two metal layers [structure A, Fig. 6(a)], which is used for ordinary two-level interconnects, and a pad stack structure with a via-contact array in BCB film [structure B, Fig. 6(b)]. To evaluate the reliability of the two structures, we employed a wire pull test in which the bond wire was pulled with a hook. Table I shows the results. For all samples, the failure mode was bond wire breaking and there was no bond pad peeling. Furthermore, good pull-off-forces of over 3.0 g were obtained in structure B. On the other hand, structure A had poor pull-off-force characteristics. The poor reliability for structure A is thought to result from the large step height of over 10 μm between the edge and the center in the top pad metal. Then, we employed structure B.

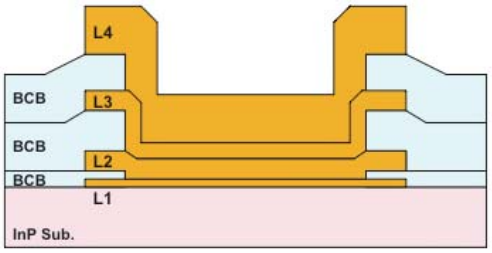

Fig. 6(a). Cross-sectional view of the pad stack structure without BCB films between two metal layers.

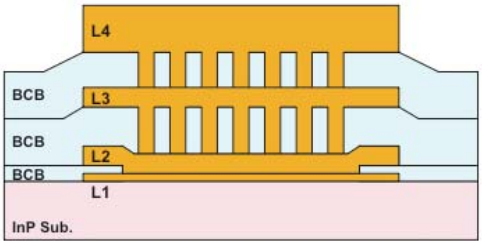

Fig. 6(b). Cross-sectional view of the pad stack structure with via-contact array.

Table I
Results of wire pull test.

Structure	Max.	Min.	Average	STD
Fig. 6(a)	3.4 g	1.8 g	2.1 g	0.7 g
Fig. 6(b)	3.9 g	3.0 g	3.3 g	0.3 g

RESULTS

We investigated the DC characteristics of two kinds of interconnect TEGs: plated Au line and via-contact chain. Good standard deviation of 3% was obtained from electrical resistance measurements for Au line TEGs with 5-μm thickness, 6-μm width, and about 1-mm length. Furthermore, good standard deviation of 2% was obtained from electrical resistance measurements for via-contact chain TEGs with 756 contacts, which have a diameter of 4 μm.

We investigated the RF characteristics of three kinds of microstrip line structures: the signal line of the 4th metal layer on the ground line of the 3rd metal layer (S4G3), the signal line of the 3rd metal layer on the ground line of the 2nd metal layer (S3G2), and the signal line of the 4th metal layer on the ground line of the 2nd metal layer (S4G2), as shown in Fig. 7. Figure 8 shows the dependence of the line loss on the characteristic impedance at 10 GHz. There is good agreement between the measurement results for S4G3 and S3G2, both of which have 5-μm-thick BCB film between the signal and ground lines. In addition, for S4G2

with 10-μm-thick BCB film between the signal and ground lines, we obtained a low loss of 0.1 dB/mm at 50 Ω. In addition, the S4G2 allows us to achieve high-characteristic-impedance (up to 90 Ω) TFMS lines, which are very useful to make compact and high-performance switch ICs.

We conclude that this technology will set the stage for the next-generation of compact switch ICs by offering circuit designers greater design flexibility and higher circuit integration.

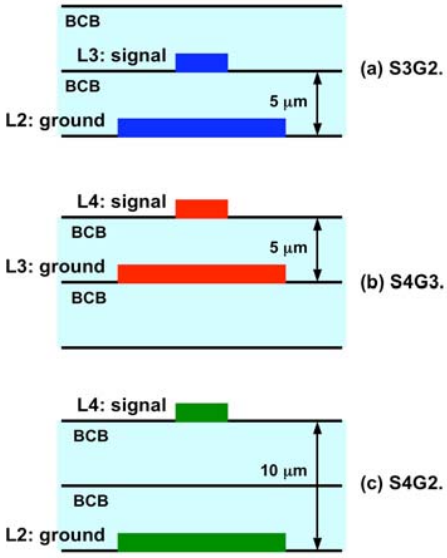

Fig. 7. Three kinds of TFMS line structures.

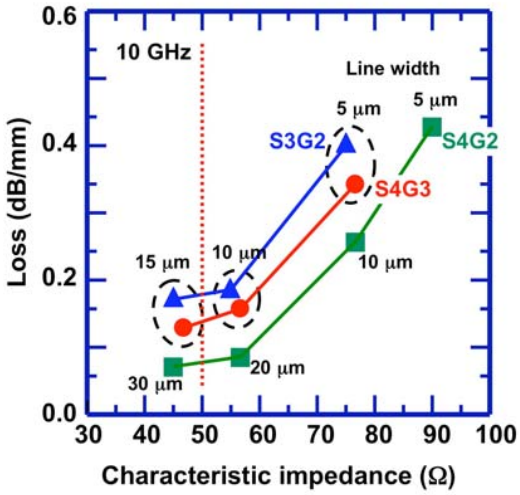

Fig. 8. Dependence of loss on the characteristic impedance for the three TFMS line structures.

CONCLUSIONS

We have been developed an advanced four-level interconnect technology to make high impedance ITLs with a low crosstalk in compact switch ICs using InP HEMTs. Via-holes with the minimum diameter of 4 μm were formed successfully in BCB film with a thickness of 5 μm by RIE with a photoresist mask using O_2/CF_4 gas and high pressure of 5 Pa. Thick Au layers with good thickness uniformity were formed by selective electroplating with low current density of 5 mA/cm^2. A pad stack structure with a via-contact array achieved better bonding reliability than a pad stack structure without BCB film between metal layers. Measured RF characteristics of TFMS lines indicated the usefulness of this technology in compact switch ICs.

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ACRONYMS

BCB: BenzoCycloButene
HEMT: High Electron Mobility Transistor
ITL: Interconnect Transmission Line
RIE: Reactive Ion Etching
TEG: test element group
TFMS: Thin Film MicroStrip