High Yield, Highly Scalable, High Voltage GaInP/GaAs HBT Technology

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Abstract

Based on a power high-voltage (HV) HBT technology the successful down scaling towards low-power devices for mixed signal integrated circuits is described. Stress effects and mechanical stability issues required processing adaptations. High yields of 99.8 % for 3x30 μm^2 and 99.0% for 2x10 μm^2 HV-HBTs were achieved. This allows for fabrication of complex integrated circuits with several hundreds of transistors monolithically combining power and digital circuit parts.

INTRODUCTION

GaAs-based heterojunction bipolar transistors (HBTs) have been used for a wide range of microwave applications. Especially, the potential of GaAs HBTs with regard to power amplifiers for levels beyond 10 W has been verified, e.g. for application in base stations. This requires highly linear HBT power cells, which can be operated at collector-emitter voltages around 26V. Due to its superior reliability high performance HBT power cells provide specific solutions until new wide-band-gap technologies become really available [1].

We have developed GaInP/GaAs HBTs matching such high bias requirements (high-voltage HBT: HV-HBT) as already reported in [2, 3]. Currently, a mature high-voltage HBT processing is available at FBH: devices with 3µm GaAs collector and breakdown voltages BV_{CBO} higher than 70 V are suitable for applications in the 1 - 3 GHz frequency range. Proprietary flip-chip mounted unit power cells with an emitter area of 4000 µm² deliver output power levels higher than 10 W at 26 V with 12 dB gain and high efficiency (PAE > 60%) at 2 GHz [3]. The high reliability of HV-HBTs was proven by accelerated lifetime measurements as shown in fig.1.

For a novel base station amplifier approach it was necessary to combine the power HV-HBTs with a digital circuit part. In order to avoid hybrid mounting we decided to use the HV-HBT technology for digital circuits, too.
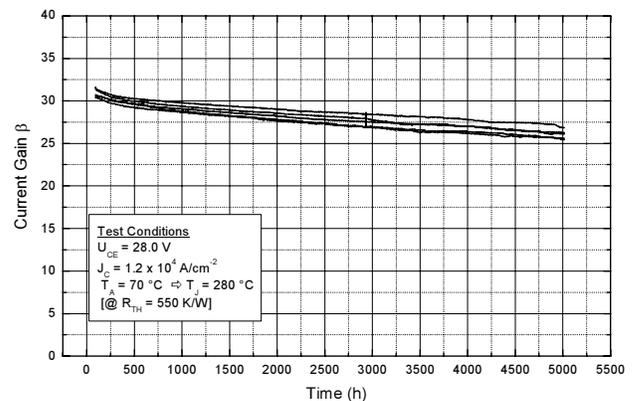

Fig. 1: Reliability measurement on HV-HBTs (3x30 µm²).

In this way monolithic integration of high-voltage (~26 V) power cells together with low-voltage (~3 V) digital circuits becomes feasible. However, the power devices, which are of large size and have thick Au thermal shunts on top, have to be combined with transistors of very small dimensions for the digital part. This is a challenging situation for the process.

EXPERIMENTAL

The high voltage HBT structures (HV-HBTs) are grown in-house on 100 mm GaAs substrates in an MOVPE reactor. The layer structures mainly consist of a 700 nm GaAs subcollector layer ($n=5x10^{18}cm^{-3}$), an up to 3500 nm thick GaAs collector layer (lowly doped in a region of 4 - $6x10^{15}$ cm^{-3}), a 100 nm GaAs base layer ($p=4x10^{19}$ cm^{-3}), a 40 nm $Ga_{0.51}In_{0.49}P$ emitter layer ($n=5x10^{17}$ cm^{-3}), and GaAs and InGaAs contact layers. Si and C are used for the n-type and p-type doping, respectively. Higher resistance layers are included in the HBT structure as emitter ballast in order to increase the electrical and thermal stability of the device.

The HBT process technology is based on a two-mesa approach in order to access the base and the collector layers. Interconnections are made by Ti/Pt/Au metal and 3.5 µm thick electroplated Au air bridges. For power cells emitter thermal shunts are formed by a 20 µm thick electroplated Au layer.

In the first technology development step we scaled the HV-HBTs down to emitter areas of 3x30 µm², 2x30 µm², 2x15 µm² and even 2x10 µm². Fig. 2 shows a group of the smallest HBTs just after the collector metallization. Despite of the reduced dimensions the wet etching of the thick collector layer was successful after optimization. Fig. 3 shows a mapping of the breakdown voltage of 2x10 µm² PCM devices (1 HV-HBT per shot). Full collector-base breakdown voltage of 70 V was obtained for all devices. Furthermore, this result confirmed that the smallest HV-HBTs can be fabricated with a yield well beyond 90% despite of the very high device topography (~6 µm).
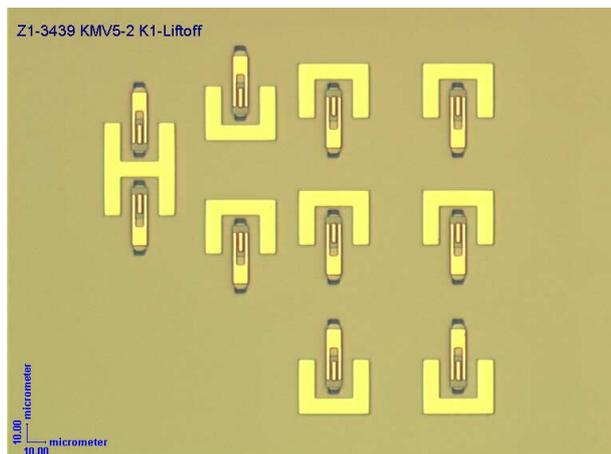
For a complex integrated circuit with several hundreds of devices, however, a yield of better than 99 % is required to ensure functionality. In order to determine the genuine HV-HBT yield we included a special monitoring stripe on the wafer that consists of a large number of single devices only.

Fig. 4 shows the position of the "yield stripe" on a 100 mm wafer. The stripe is formed by 10 stepper lithography "shots" along the wafer diameter. Each shot contains high numbers (24 - 100) of single devices for a given emitter size arranged as tight as possible.

Our standard HV-HBTs use symmetrical air bridges. For the digital circuits it was necessary to use non-symmetrical variants connecting the device from one side only. In order to make a distinct yield determination both types of devices were included to the "yield stripe": odd numbered "shots" comprising the standard symmetrical devices and even numbered "shots" of the non-symmetrical ones. The viewgraphs in fig. 4 visualize this arrangement.

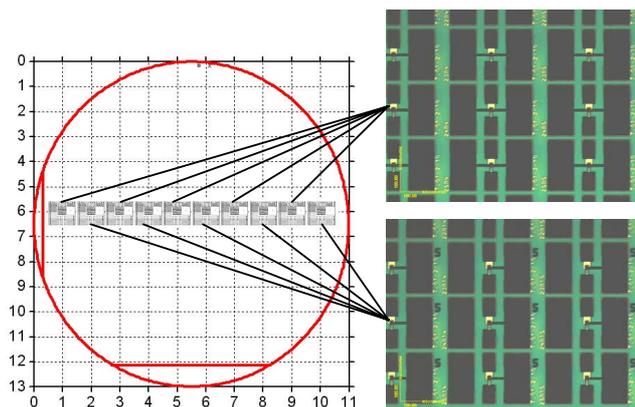Fig. 2: Detail view of a HBT group in a digital circuit (2x10 µm²).

Fig. 4: Arrangement of stepper shots for yield evaluation on 100 mm wafer. The two types of HBTs: with symmetric or non-symmetric air bridge, are highlighted.

YIELD DETERMINATION AND OPTIMIZATION

DC device parameters like current gain and ideality from Gummel-plot, output characteristics and breakdown voltages were obtained by mapping each of the device type on the "yield stripe".

Fig. 5 shows a yield result for the smallest HBTs (2x10 µm²) obtained before processing optimization. The current gain β was mapped with failure criterion β < 15 since all of the non-functional devices had no current gain. The over-all yield was only around 50%. Interestingly, the devices with non-symmetrical air bridge (even shot numbers) are severely affected by failures giving a low yield value of 11.6%. On

Fig. 3: 2x10 µm² HV-HBT: breakdown voltage map.

the other hand, the symmetrical air bridge improves the yield to 94%. This effect can be clearly seen in Fig. 5 comparing the odd and even numbered shots.

All of the failed devices exhibited no emitter contact while the base-collector diode worked properly. Thus, the emitter contact got lost during the air-bridge processing.

Table I summerizes the impact of emitter area scaling on the yield measured on several wafers. The failures described above and thus the strongly limited yield arose only for the two smallest device sizes. HV-HBTs with 30 μm long emitters gave in all cases high yield values in excess of 99% (Fig. 7).

Obviously, the devices with shorter emitter fingers were adversely affected by the air bridge processing. As a possible mechanism it can be assumed that mechanical strain in or on the air bridge tears off the plated Au layer from the emitter.

Severe underetching of the emitter layers in case of the smallest devices could lead to worse mechanical stability of the air bridge. However, since in our process the emitter etching already was optimized towards low undercut, further reduction of etching times towards the edge of the processing window gave no yield improvements.

Another point of considaration was the plating processing. Since in our case the plating was performed at elevated temperature, the plated Au layer is strained due to the large difference in thermal expansion coefficients for Au and GaAs. On fully plated test wafers the thermally induced tensile strain was determined to be in the range of 50 MPa. On the other hand, this strain value can be expected from strain calculations for this layer system. Thus, no additional strain is caused by the plated Au layer, and only the thermal expansion effect has to be taken into consideration.

Further impact on air bridge strain can be expected from resist deposition and possible resist change during the plating procedure. Last but not least, the layout and proper design of the air bridge have strong influence on air bridge stability.

After these investigations we were able to optimize our HV-HBT processing towards improved yield of short emitter devices. Fig. 6 shows the obtained yield for the smallest HV-HBTs (2x10 μm²) after processing optimization. Despite of few failures a high yield of 99% is achieved. Furthermore, there is now no yield difference between symmetrically and non-symmetrically air-bridged devices which is obviously the most important result for fabrication of circuits.
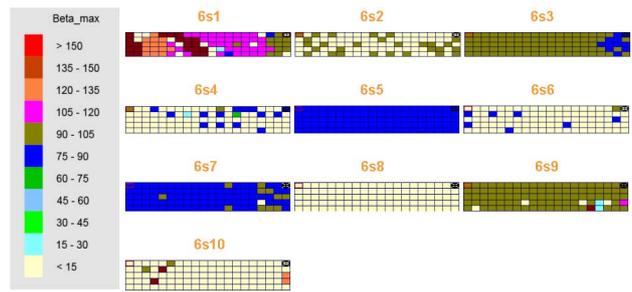

Fig. 5: Current gain map of 990 HBTs (2x10 μm²) along the diameter of a 100 mm wafer (divided in four segments for the sake of visuality) before processing optimization (473 failures giving yield of 52.2%).
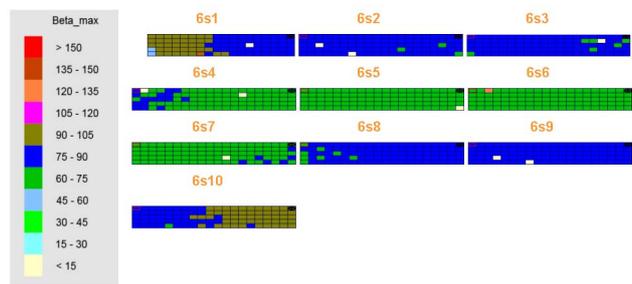

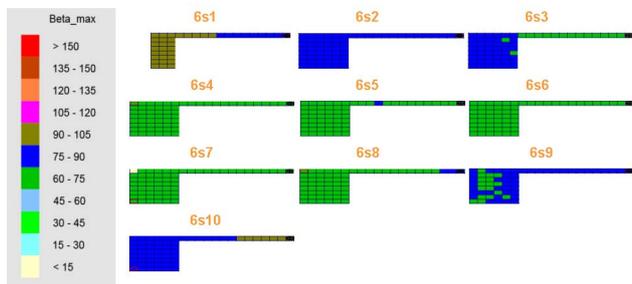Fig. 6: Current gain map of 990 HBTs (2x10 μm²) after processing optimization (10 failures giving yield of 99.0%).

Fig. 7: Current gain map of 604 HBTs (3x30 μm²) after processing optimization (1 failure giving yield of 99.8%).

Fig. 7 confirms that the very high yield in the upper 99% range was still maintained after changes in device processing.

Table 1 gives the yield results in dependence on the HBT size before and after process optimization. The clear improvement in yield was achieved especially for smaller HV-HBTs.

TABLE I
HV-HBT YIELD IN DEPENDENCE ON EMITTER SIZE

emitter area (μm^2)	yield (%)	
	non-optimized	optimized
3 x 30	99.8	99.8
2 x 30	99.4	99.8
2 x 15	52.2 - 98.9	98.9
2 x 10	48.2 - 79.6	99.0

FABRICATION OF MIXED SIGNAL CIRCUITS

Based on the yield study an optimized HBT size was determined for circuit design. Circuits with integrated digital and power parts consisting of large numbers of devices (from 100 up to 670 HV-HBTs) have been manufactured. Fig. 8 shows an example of a fabricated mixed signal (digital and power) circuit.

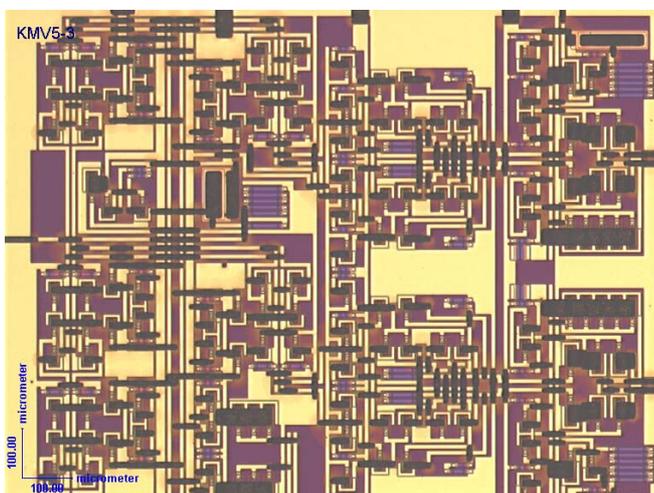The circuits have proven its functionality at data rates as high as 2 GB/s.

Fig. 8: Part of a finished mixed signal (digital and power) circuit.

CONCLUSIONS

We have shown that starting with a high-power HV-HBT the successful downscaling towards low-power device is possible. With shrinked device dimensions stress effects and mechanical stability issues become crucial. In this paper it is described how careful device evaluation and process optimization can be performed in order to maintain high yield.

ACKNOWLEDGEMENTS

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ACRONYMS
HBT: Heterojunction Bipolar Transistor
HV-HBT: High Voltage HBT
PCM: Process Control Monitor
DC: Direct Current