Dry Etch Development for a Dual, Front and Backside, processing of II-VI Compound Semiconductors

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Abstract

A set of methods were developed to allow for dual-side plasma processing of the electro-optical II-VI compound semi-conductor HgCdTe. Conventionally, HgCdTe is processed on a single side. The dual side processing of HgCdTe is an enabler to produce detectors beyond the complexity of the current state of the art. The research performed has allowed innovations in wafer bonding methods, substrate removal, infrared mask aligning methods, and new plasma processes. These innovations will allow the productions of infrared detectors and other electro-optical detector designs.

Introduction

HgCdTe is a II-VI compound semiconductor. This semiconductor has a direct bandgap that can be adjusted from -0.26 bandgap for HgTe to 1.61 eV @ 77K for CdTe by changing the ratio of Cd to Hg. This property of HgCdTe makes it an ideal photovoltaic semiconductor for infrared detection. Resent research into HgCdTe has allowed the growth of complex structures allowing multiple photovoltaic detection bands to be grown into a single structure, example in figure 1. Multiple detection bands together with smaller pixels provide better resolution both spatially and spectrally. This allows better detection and resolution.

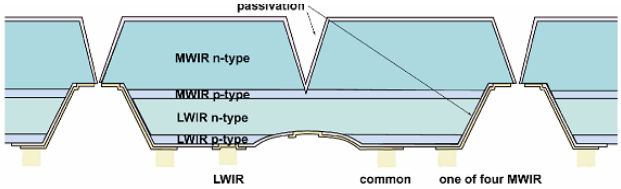


Figure 1. Example of two pixel array with Dual Side Processing.

The next generation HgCdTe focal plane arrays (FPAs) will have absorber layers greater than 30 microns thick, with as four or more p-n junction per-pixel may be desired. Contact vias for metallization to multiple diodes will be needed. Single sided processes limit the number of active device layers that can be accessed through these layers. Dual side plasma processing will enable designs that allow for a greater number of vias to be produced and deeper pixel delination through these thick absorber layers. It will also allow complex structures like microlens and anti-reflective structures to be added to layers easily.

The majority of the research into dual-side processing of HgCdTe is in dry etch development. Argon-hydrogen plasmas, generated in inductively coupled plasma (ICP) reactors, have been demonstrated to be effective in etching CdTe, CdZnTe, and HgCdTe materials for focal plane array applications[1-4]. Several studies have also reported the effect high density "dry" ECR plasmas have on HgCdTe epitaxial properties[5-14]. However, ICP plasma processing, for use in HgCdTe, is still maturing and continued research is needed[4,7,14]. Producing plasma processes that can be used to delineate pixels, etch vias, clean surfaces, and even produce epi ready surfaces would allow HgCdTe to become much more manufacturable and even replace wet chemical etch in the factory. To take advantage of these advances in plasma processing methods need to be developed. This paper will outline a set of methods that enable complex structures to be processed in II-VI materials.

Process Flow

The standard process flow of a HgCdTe based optoelectronic detector is exhibited in figure 2 and is as follows. It starts with a substrate, usually a latticed match CdZnTe or another alternate substrate like Si with appropriate buffer layers. HgCdTe is then grown on the substrate using molecular beam epitaxy (MBE), liquid phase epitaxy (LPE), or metal organic chemical vapor deposition (MOCVD). Passivation can then perform by depositing CdTe, eventhough CdTe is a

semiconductor it band gap is very large and insulator-like compared to the HgCdTe. The surface is then plasma processed to delineate and/or form vias. This is follow by metallization and then hybrid bump bonding to a readout circuit. The substrate is removed, usually through a chemical mechanical process. The backside plasma process can then be performed followed by appropriate metallization and passivation. Finally advance structure like microlenses or anti-reflective structures can then be produced on the surface.

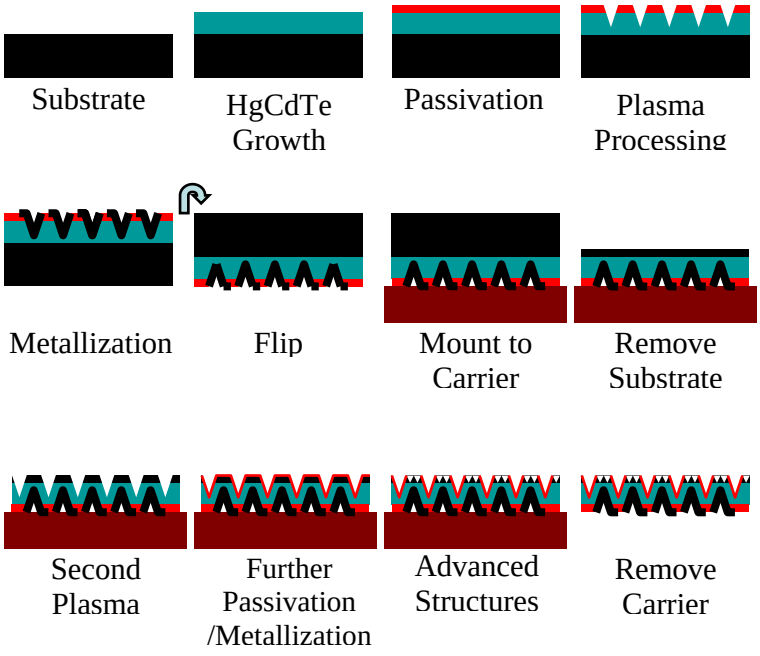
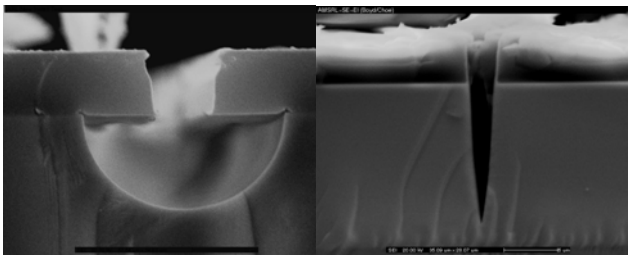


Figure 2. Example Dual Side Plasma Process Flow.

Six areas of research have been identified as necessary to produce a dual side process. These are a follows: Trench Etch, Passivation and Metallization, Wafer Bonding, Substrate Removal, Back Side Processing, Individual processes brought together.

Trench Etch

ECR (electron cyclotron resonance) and ICP (inductively coupled plasma) plasma processes were researched, together with ultra thick photoresist processes, to produce the trench delineation, figure 3. These argon:hydrogen based plasma processes allow for trenches to be produced that are greater than 15 microns deep with a 5:1 aspect ratios. A semiconductor to photoresist selectivity of 10 or greater is possible with the use of standard photoresists and these plasma processes, ref 5-6. However ever as these trenches become deeper (greater that 2:1 aspect ratios) severe etch lag can occur. A reduction in process pressure and increases in sample biases can help off set this problem. Additionally HgCdTe has a <90 C processing temperature limit, making temperature cures during photoresist development difficult. To offset these problems a 10 micron thick photoresist was researched and successfully produced to reduce photoresist erosion issues in processing very deep structures. A contrast enhancement layer is used to allow for greater exposure times needed to develop this thick resist, and a backside anti-reflective coating is used to limit light scattering. This thick photoresist technology together with plasma processing will allow trenches greater than 30 microns deep to be produced.



a) b)

Figure 3 a) Trench formed in HgCdTe using standard wet chemical processes. b) Trench formed HgCdTe using new plasma parameters and new resist processes. Width = 2.91 microns, Depth = 15.74 microns, and Aspect Ratio = 5.41.

Metallization

These materials must be able to adhere to the trench etched parts while allowing conformal coverage on both the top and inside the trench delineation. These metals must also not induce stress into the semiconductor. A Metallization of 100ATi/4000A Au using e-beam deposition was found to adhere well to the HgCdTe and make a good ohmic contact to the p-type HgCdTe.

Wafer Bonding

The front side processed wafers need to be to a carrier so that the backside can be processed. A variety of materials was tested as a possible wafer

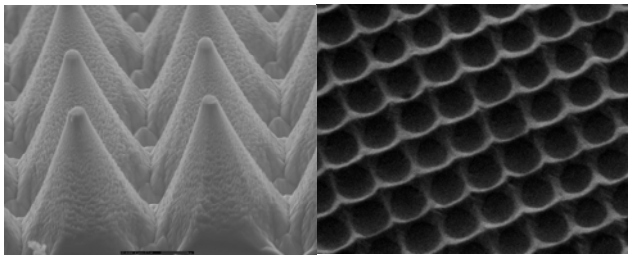
bonding material. It has been found that photoresist and Bee's Wax were easy to work with and provided enough bonding to allow substrate removal. Epoxy is very hard to remove. Apiezon M allows the sample to move on the carrier wafer during substrate removal. However, Epoxy was finally used as it is able to survive the substrate removal step and is compatible with hybrid bump bonding usually used in connecting HgCdTe detector arrays to their Si readout circuits.

Substrate Removal

Initial experiments with mechanical polishing left a non-planer surface, which is undesirable. A bromine methanol chemical-mechanical removal was found to work leaving a uniform-planer surface.

Back Side Processing

After substrate removal backside processing can take place. As far as trench delineation is concerned, the process is similar to that of the frontside plasma processing. However one issue is different. Photoresist patterns need to be aligned to those on the frontside. An infrared aligner, performed by Rockwell Scientific, allowed the backside pattern to be aligned with the frontside patterns. In addition to backside trench delineation, other plasma processes can be performed to create advanced structures like anti-reflective structures, microlenses, and diffraction gratings, figure 4. These structures are produced by using gray scale masks during the photoresist exposure and controlling the selectivity of the semiconductor to resist removal during the plasma process by varying the argon:hydrogen ratio and the pressure of the plasma.



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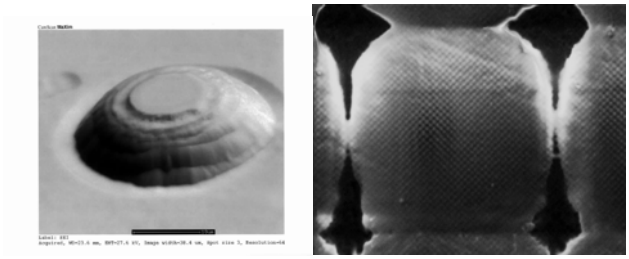

c) d)

Figure 4. Possible Backside structures a) and b) Example of a Anti-Reflective Structure produced at night vision laboratory c) Example of a Microlens produced at night vision laboratory d) Image of Photoresist anti-reflective Embedded Microlens Structures

Final Device

Figures 5 and 6 demonstrate the dual side etch process, all the earlier process steps were brought together.

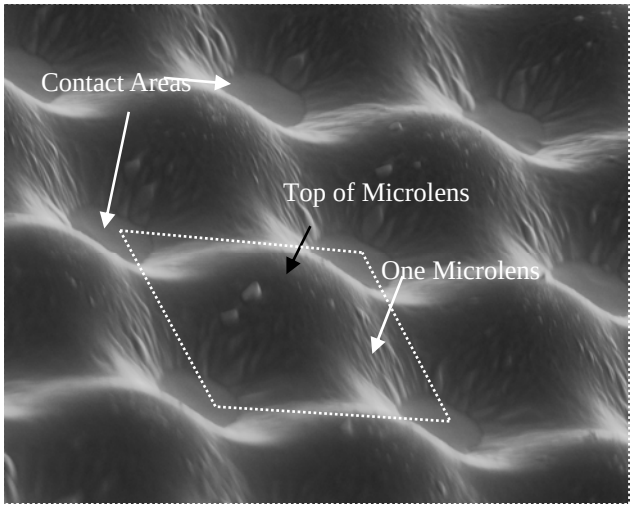

Figure 5. A 30 deg. view scanning electron micrograph of the backside of a dual side etches structure.

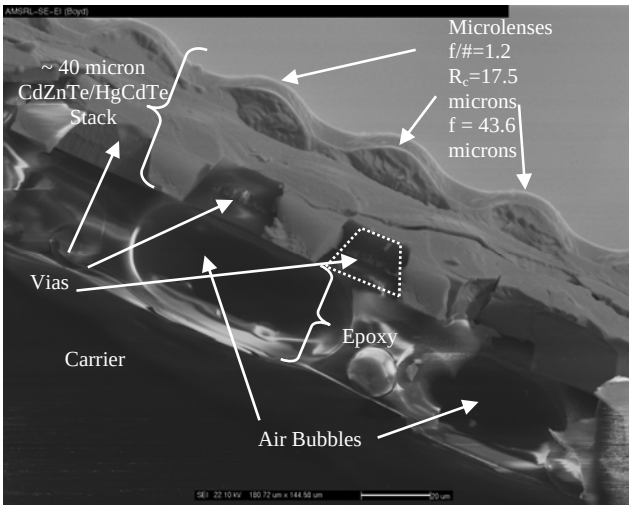

Figure 6. A Side View Scanning Electron Micrograph of a dual sided etched structure. Note: backside on the top with the microlenses.

Conclusion

A set of methods were developed to allow for dual-side plasma processing of electro-optical II-VI compound semi-conductor. Six areas of research have been identified as necessary to produce a dual side process. These are a follows: Trench Etch, Passivation and Metallization, Wafer Bonding, Substrate Removal, Back Side Processing, and final integration of the processes. These six areas have been examined and prototype devices have been produced using these developed processes.

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