Deep Submicron GaN-based Heterostructure Field Effect Transistors with InGaN Channel and InGaN Back-barrier Designs

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Abstract

We developed a double-recess etching process and a new Digital-Oxide-Deposition (DOD) technique to fabricate 180nm low-threshold GaN Metal-Oxide-Semiconductor Double Heterostructure Field Effect Transistors (MOS-DHFET). Two device layer structures, InGaN channel design and InGaN back-barrier design, were employed to improve the confinement of Two-Dimensional Electron Gas (2DEG) and mitigate the short-channel effects. The devices exhibited high drain-currents of 1.3 A/mm and delivered RF powers of 3.1 W/mm at 26 GHz with a 35 V drain bias. A cutoff frequency of about 65 GHz and a maximum oscillation frequency of 94 GHz have been achieved. The subthreshold swing and the Drain Induced Barrier Lowering (DIBL) in those devices are less than 75 mV/decade and 80 mV/V, respectively. To further improve the confinement of 2DEG, we combined and optimized the InGaN channel design with the InGaN back-barrier design. We also developed a selective doping technique to reduce the high electrical field around the recessed gate and improve the electric field profile in the ungated drift region for supporting high voltage. In addition, the selective doping technique also leads to the reduction of parasitic drain and source resistance in deep-submicron GaN Heterostructure Field Effect Transistors (HFETs) and consequently improves the device RF characteristics.

INTRODUCTION

In the past decade, significant research efforts have been invested on GaN Heterostructure Field Effect Transistors (HFETs) due to their promising application potential in wireless communication, high RF power circuits, and avionics. The performance of GaN HFETs has been largely improved from a humble start in 1993 [1] to a more mature and nearly commercialized stage. Over 30 W/mm output microwave power density have been reported in the frequency range of 2-8 Hz [2]. Now the focus of the research efforts is shifting to higher frequencies [3, 4].

The reduction of the gate length is the most efficient way to increase the operational frequency of GaN HFETs. In the standard design of GaN Heterostructure Field Effect Transistors (HFETs), if the ratio of gate length to the AlGaN barrier thickness is below 20-30 as the gate length of HFETs continues to shrink and reach the deep submicron or nanometer scale, the device performance could be dramatically impaired by short channel effects, including large threshold-voltage shift, soft pinch-off due to the injection of hot electrons into the buffer at high electrical field around the gate, high subthreshold current and increased output conductance, etc. Those adverse effects are mainly caused by the poor confinement of 2DEG at the hererojunction interface and the reduction of gate modulation efficiency at shorter gate. Electrons can become extremely hot in the high electrical field around the gate of the short-channel GaN HFETs. Simulation results show that the temperature of the hot electrons could be over 2500K, and could easily escape from the potential well into the buffer without any difficulty. Thus, in the standard short-channel HFETs, the 2DEG has poor confinement in the device channel and is extended into the buffer.

Although recessed gate structures are commonly adopted in GaN HFETs to improve the gate modulation efficiency, however, short channel effects in the devices still remain, the high electric field around the recessed gate will cause the transistor to break down prematurely. In addition, the transistor could not support very high drain bias partially due to the bad electric field profile in the ungated drift region between the gate and the drain. The common recessed gate structures normally also have passivation problems around the corner of the recessed gate.

In the standard GaN HFETs, the gate leakage could cause severe reliability issues as the devices are subject to a long term electrical stressing. Therefore, it is preferable to dramatically reduce the gate leakage currents in GaN HFETs, making them promising for use in commercial applications. In the past, we inserted an ultra thin oxide layer into the standard structure of GaN HFETs for suppression of gate leakage. We have successfully demonstrated Metal-Oxide-Semiconductor Double Heterostructure Field Effect Transistors (MOS-DHFETs) operating at 2 GHz with an 1 µm gate [5]. Lower gate leakage, at least 2-3 orders less than conventional HFETs,

was achieved in these insulating gate devices. The reduction of the gate leakage current dramatically improved the stability of the devices [6]. We have also demonstrated stable CW operation of GaN-AlGaN MOS-HFETs at a microwave power density of 19 W/mm for over 100 hours. In comparison, the GaN-AlGaN HFETs without the ultra-thin oxide layer in the same lot have a 30% drop in the microwave power density within 30 hours [7].

In this work, we adopted a double recessed gate structure formed by a double-recess etching process to increase the gate-to-barrier aspect ratio and eliminate the passivation problems at the corner of the recessed gate. We used a new Digital-Oxide-Deposition (DOD) technique to deposit an ultra-thin gate oxide of 40 Å under the foot of the gate for suppression of gate leakage. Two device layer structures, InGaN channel design and InGaN back-barrier design, were employed to improve the confinement of 2DEG and mitigate the short-channel effects. We combined and optimized the InGaN channel design with the InGaN back-barrier design to further increase the confinement of the 2DEG. We also employed a selective doping technique to reduce the high electrical field around the recessed gate and improve the electric field profile in the ungated drift region for supporting high voltage.

DEVICE DESIGNS, RESULTS AND DISCUSSIONS

The device layer structures that we used for GaN MOS-DHFETs are (1) InGaN channel design, and (2) InGaN back-barrier design. In the InGaN channel design, a thin InGaN channel layer is sandwiched between the AlGaN barrier and the GaN buffer layers of the heterojunctions (AlGaN/ultra-thin AIN/InGaN/GaN buffer) [8]. Due to a large electron affinity of InN (5.8 eV), the InGaN channel layer forms a deep potential well and a discontinuity of conduction band at the interface of InGaN and GaN buffer, thereby effectively confining the electrons in the device channel. In the InGaN back-barrier design, a thin InGaN back-barrier is inserted between the GaN channel and the GaN buffer (AlGaN/ultra-thin AlN/GaN/InGaN back-barrier/GaN buffer) [9]. The InGaN back-barrier creates an effective conduction band discontinuity of approximately 0.2 eV between the GaN channel and the GaN buffer. Thus, the 2DEG could be well-confined in the device channel. In both designs, an ultra-thin AlN layer is inserted between AlGaN and GaN. It was known in the past that the ultra-thin AlN layer offers significant advantage over the conventional AlGaN barrier, simultaneously providing higher sheet charge density and mobility and reducing the gate leakage.

The GaN MOS-DHFETs with two device designs were grown by metalorganic chemical vapor deposition at 76 Torr. A 50 nm AlN buffer layer was first grown on the substrate at 1000 °C, and then a 0.4 µm insulating GaN layer was followed after the AlN buffer. For the InGaN channel design, the growth temperatures for the GaN buffer and the AlGaN barrier layers were 1000 °C and 1100 °C, respectively. For the InGaN back-barrier design, the GaN channel was deposited after the growth of InGaN epilayer. The growth temperature of the GaN channel was reduced from 1145 °C to 920 °C to reduce the Indium out-diffusion. The InGaN layer was grown at 820 °C to assist with the In incorporation. The In composition in the InGaN layer was calibrated using X-ray diffraction and photoluminescence analysis and is about 10%. A total charge density of around 1.5×10^{13} cm^{-2} and a mobility of 1240 cm^2/V-s were obtained by Hall measurements. The AlGaN barrier had an aluminum alloy composition of 30 %. The thickness of the AlGaN barrier was around 200 Å. Device mesas were formed by reactive ion etching for the device isolation. Ti(200 Å)/Al(500 Å)/Ti(200 Å)/Au(1500 Å) were used for source and drain contacts. The Pt/Au Schottky gates were defined after a double recess etching process and then metalized.

The device processing started with mesa isolation. The mesa etch was achieved by an ICP system. Thereafter, the ohmic contacts (Ti/Al/Ti/Au multilayer) were deposited and annealed at 800 °C for 1 min in nitrogen ambient. In order to increase the gate-to-barrier aspect ratio, we developed a novel double recess etching (DRE) process in the device fabrication. In this process, a 0.35 µm wide trench defined by E-beam lithography was formed by the ICP system at 75 V DC bias for the first recess. The depth of the trench for the first recess was 40 Å. After the first recess, the second recess was done by the ICP system at 55 V DC bias in the center of the first trench. The trench for the second recess has a width of 0.2 µm and a depth of 40 Å, which was aligned in the center of the first trench. After this double recess etching process, a high-quality and extremely uniform 30-40 Å SiO$_2$ as the gate-insulator was deposited using a novel digital-oxide-deposition (DOD) technique at 300 °C [10]. Finally 0.18 µm wide (Ni/Au) gates were also fabricated by another e-beam alignment step. They were positioned within the second recess etch trench using new alignment marks defined by e-beam lithography. After that, probe contacts were deposited and devices were passivated by silicon nitride layers.

The DC characteristics of InGaN channel and InGaN back-barrier MOS-DHFETs were measured by an Agilent 4155B Semiconductor Parameter Analyzer. The small signal and RF power measurements of those devices were performed thereafter. The devices exhibited high drain-currents of 1.3 A/mm and delivered RF powers of 3.1 W/mm at 26 GHz with a 35 V drain bias. A cutoff frequency f_T of about 65 GHz and a maximum oscillation frequency f_{max} of 94 GHz have been achieved. As shown in Fig. 1, the InGaN channel MOS-DHFETs yielded a sub-threshold slope S as low as 35 mV/decade and a Drain Induced Barrier Lowering (DIBL) of 80 mV/V while the InGaN back-barrier MOS-DHFETs exhibited a sub-threshold slope S of 75

mV/decade and a DIBL of 40 mV/V. From the transfer characteristics, we can conclude that both the InGaN channel design and the InGaN Back-barrier design effectively confine the electrons in the device channel.
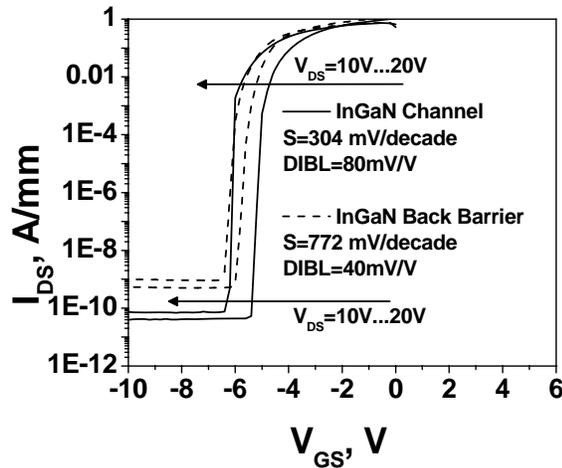

Fig. 1. Transfer Characteristics of InGaN Channel and InGaN Back-Barrier MOS-DHFETs.

In order to further improve the confinement of the 2DEG and prevent electrons in the 2DEG from spilling over into the GaN buffer, we combined and optimized the InGaN channel design with the InGaN back-barrier design to confine the electrons within 50 nm near the heterojunction interface as shown in Fig. 2.

We used the SENTAURUS TCAD simulator from SYNOPSYS, Inc. to optimize the device design. As seen from Fig. 2 (b), the InGaN channel has a deep potential well due to the large electron affinity of InN (5.8 eV), thereby effectively confining the electrons in the well. The InGaN back-barrier creates an effective conduction band discontinuity of 0.1 ~ 0.3 eV between the channel and the buffer approximately. Thus, the electrons are prevented from being injected into the buffer by the back-barrier. The thickness of InGaN channel and InGaN back-barrier has to be optimized since thicker InGaN channel will counteract the function of the back-barrier while thicker back-barrier will generate a parasitic back channel. Fig. 3 shows the electron density in the optimized design as compared to other device structures. The results show that the confinement of 2DEG in the device channel is largely improved in the optimized design.

We also developed a selective doping technique to reduce the high electrical field around the recessed gate and improve the electric field profile in the ungated drift region for supporting high voltage. The selective doping around the drain and the source regions in HFETs is achieved by deposition of a thin layer of silicon oxynitride (SiON) followed by 650 ℃ anneal in a forming gas ambient for 5

minutes. The selective doping technique with low annealing temperature does not cause damages to the device channel and is more superior than the conventional ion implantation method that requires an above-growth temperature (>1100 ℃) annealing to reduce the implantation induced defects.
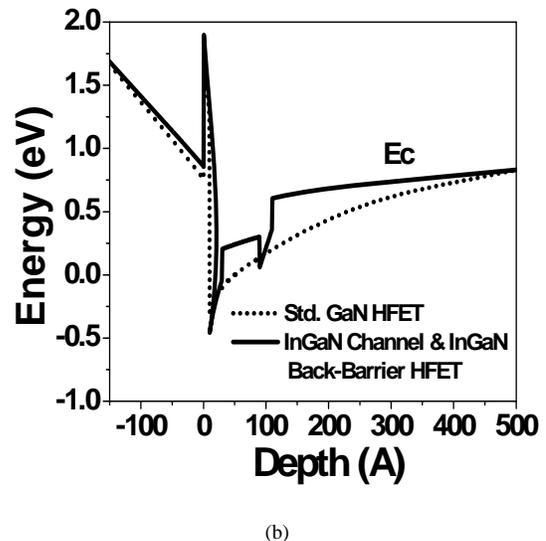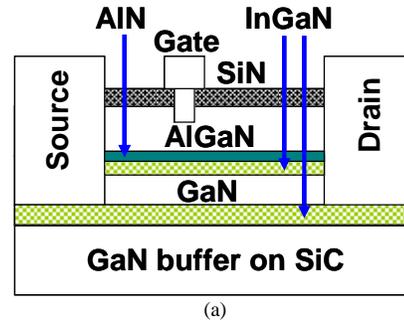

(a)

(b)

Fig. 2. GaN HFET with an InGaN Channel and an InGaN Back-barrier. (a) The device layer structure; (b) The band diagram.
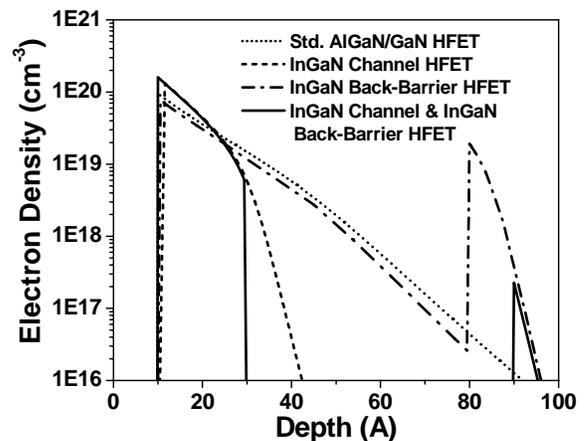

Fig. 3. Electron Density Distribution in GaN HFETs with different device designs.

The device structure of HFETs with selectively-doped zones is shown in Fig. 4. Using the SENTAURUS TCAD simulator, we simulate the electrical field profile in a deep submicron GaN HFET with selective doping regions. For a deep submicron HFET with a gate length of 100nm and a 1.5μm source-drain spacing, the optimized doping level near the drain region within 25 nm around the heterojunction interface is about 1×10^{18} cm^{-3}. At this doping level, the electric field around the gate edge is reduced; the electric field profile in the ungated drift region has a trapezoidal shape as seen in Fig. 5 and can support higher voltage, as compared to the electrical field profile with a triangle shape in the HFET without selectively-doped zones. However, higher doping level does not improve the electrical field profile since it pushes the electrical field in the drift region to the gate. Multiple selective doping zones can further improve the electric field profile and decrease the parasitic drain resistance. The doping level near the source region should be as high as possible to reduce the source access resistance. The reduction of parasitic drain and source resistance leads to the improvement of the device RF characteristics. In addition, the selective doping technique also has a lower parasitic capacitance than that of the field plate design.
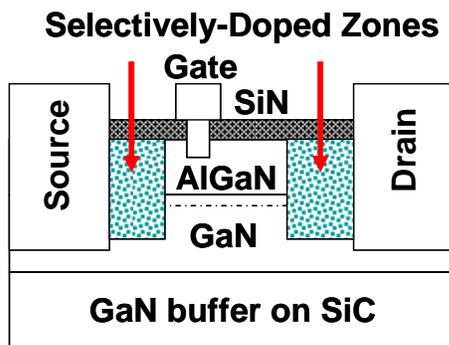

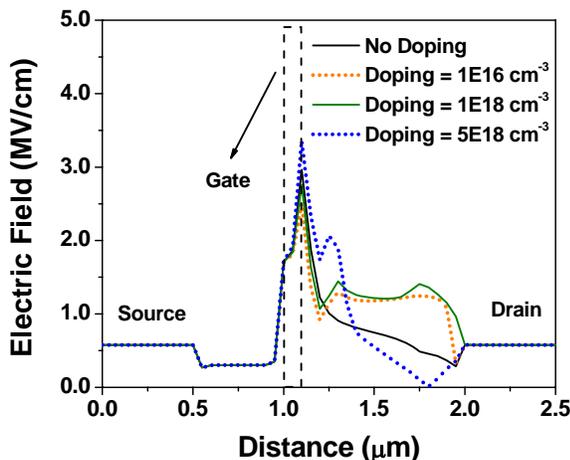Fig. 4. HFET with selectively-doped zones.

Fig. 5. The electric field profile. L_G=100 nm, V_G=-1.5 V, and V_{DS}=50 V.

CONCLUSIONS

In summary, we have successfully demonstrated 180nm low-threshold MOS-DHFETs with InGaN channel and InGaN back-barrier designs. The devices exhibited pretty decent performance. The confinement of the 2DEG is improved and the short-channel effects are mitigated in both designs. To further increase the confinement of the 2DEG, both InGaN channel and InGaN back-barrier were used in the device layer structure. Better confinement of the 2DEG was found in the optimized design. Using the selective doping technique, the electric field around the recessed gate is reduced and the electric field profile in the drift region is significantly improved. Consequently, the transistors can support higher drain voltage and have smaller parasitic source and drain resistance.

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ACRONYMS

MOS-DHFET: Metal-Oxide-Semiconductor Double Heterostructure Field Effect Transistors
2DEG: Two-Dimensional Electron Gas
DIBL: Drain Induced Barrier Lowering
DOD: Digital-Oxide-Deposition