Yield Improvement Methodology in a pHEMT GaAs Fabrication Facility

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Abstract

Shrinking feature sizes, increasing circuit complexity, and stringent RF performance requirements make achieving high yield a considerable challenge. This paper presents a method to improve yield in a pHEMT GaAs wafer fabrication facility. A practical team approach and applied technical methods to support an effective yield improvement effort are discussed. Several case studies are presented to illustrate the efforts and success of the Skyworks-Woburn GaAs Fab Yield Improvement Team.

INTRODUCTION

Multimode cell phone architectures require 6 to 10 throw RF switches. Each arm of the switch must meet stringent performance specifications for insertion loss and 3rd harmonics. Furthermore, an intermodulation distortion requirement (IMD) has been added. Despite shrinking design layout rules, the added circuit complexity results in increasing die sizes. Due to material cost implications, RF Module assembly demands known good die. Consequently, die that don't meet the performance criteria must be removed at wafer probe. The combination of these requirements makes achieving high probe yield challenging.

This paper presents the yield improvement strategy used by the GaAs pHEMT Switch Fab of Skyworks Solutions located in Woburn, MA. The strategy utilizes an engineering team dedicated to improving yield. Elements of the strategy are discussed, including skills of the team, tools utilized, and improvement techniques. Several case studies are presented to illustrate the efforts and success of the Yield Improvement Team.

DISCUSSION

YIELD IMPROVEMENT TEAM STRUCTURE AND SKILLS

There are many ways to organize a yield improvement effort. Each fab will have its own unique structure. Our team is a subgroup of the Process Engineering Group, comprised of people with diverse but complimentary skills. It is important to have a diverse group of people to obtain the benefit of unique perspective. The Team consists of a Six Sigma team leader, management sponsor, and engineers with MBE expertise, failure analysis, device, reliability, wafer processing, and operations experience. The Team serves as an interface between design and product engineers and the wafer fab Process Engineering groups. The Yield Team searches for root causes of yield loss and follows wherever the data leads. The data can point to issues in process, test, design, materials, etc. The Team follows the data and works with the engineers who are responsible for the area. Experts in the area under investigation are brought into the investigation and improvement effort. When the root cause of a yield loss mechanism is found, the solution is often straight forward. Finding the root cause is often harder than coming up with a solution.

YIELD IMPROVEMENT TEAM RESPONSIBILITIES

The basic responsibilities of the Yield Team are as follows:

- Establish a system to collect, retrieve, and analyze yield data.
    - A database of the yield information collected throughout the process is developed
    - Process data is collected at many steps in the process as material moves through the fab
    - Test data is collected at each test point in the process. Pass/fail information as well as raw data is collected for each test
    - An efficient method to query the database must be available
    - Statistical analysis software is used to analyze the data. Data from the various process steps is correlated to wafer probe, final package and module yield performance data
- Track and report yield metrics for each of the main milestone points in the manufacturing process. These metrics need to be presented weekly, monthly, quarterly, and annually. They should include a summary of the overall yield as well as the top five volume products individually. The process milestones tracked at Skyworks are:
    - MBE/EPI
    - Wafer fab
    - Pre-channel IDS
    - Post channel IDS
    - Post-gate etch current

    - Process Control Monitor (PCM)
    - Wafer probe
    - Outgoing visual inspection
- Yield bin analysis for all products combined, plus the top five volume products broken out separately; Pareto of the top three causes of yield loss at each process milestone is created.
- Identification of the critical yield limiting issues to be worked on: Because resources are limited, it is important to select the issues that if corrected, will have the largest increase on yield. This is accomplished by calculating the Yield Impact Metric (YIM). Essentially this is a multiplier of the yield loss times the wafer demand. Both present and future demand must be considered. Products/issues with the highest yield impact number are the ones to work on. Quite often, the issues that need to be worked on are obvious and there is no need for any calculations. However, when you get beyond the obvious, the YIM is a convenient way to both rationally decide what to work on, and to explain to management why you are working on what you are working on.
- Identify and eliminate the root cause of failures: Action plans and projects are initiated to identify and eliminate the root cause of failures. This is where the work is done to improve yield. Yield improvement efforts focus on the top items on the Pareto charts.
- Establish routine failure analysis (F/A) of a sample of failures from the top Pareto items:
    - Collect statistics in a database
    - Prepare and store F/A reports in a database
    - F/A will determine root cause
    - Prepare root cause summary report on a routine basis
- Create a yield model:
    - The model will include the process flow, die size, gate periphery, number of photo levels, and the gate width
    - Utilize the model to identify products that have unusual yield performance (both good and bad). Unusual yield may have a design or layout cause or process window issue

YIELD IMPROVEMENT TOOLS

The yield improvement effort requires tools to be available to the Team. This includes measurement and analytical equipment as well as software to collect, store, query, and visualize data. The tools must be easily accessible to promote their use. Measurements and data that are difficult to obtain result in drastically reduced samples sizes. Larger samples sizes increase the confidence of observed differences and allow for finer resolution. The following are lists of equipment and software need by a yield improvement team:

- Equipment
    - Microprobe station with hot/cold chuck
    - Electrical parametric measurement equipment
    - Photoemission & camera capability on the probe station microscope
    - SEM with EDAX
    - FIB for sample preparation
    - Microscope with high magnification bright field/dark field short working distance lens, and digital camera
    - Oven
    - Autoclave
- Software required
    - Database of test data
    - Database query software
    - Wafer mapping software
    - Statistical analysis software
    - PSA yield analysis. Matching PCM data to the product die surrounding each PCM [1]
    - Zonal and radial yield analysis

YIELD IMPROVEMENT STRATEGY

The strategy is simple in concept, but deceptively difficult to implement. Using software tools, the Yield Team collects and analyzes data. Trends are recognized and investigated using the software and analytical equipment. The Yield Impact Metric is used to determine which products require long term yield improvement efforts. Systemic process improvement opportunities are explored. New equipment and process changes are evaluated. Short term activities involve investigating the root cause of low yielding lots. The basic procedure followed is to identify the test parameter that failed. For example, 3rd harmonics, IMD, Idss, leakage, etc. The visual pattern of the yield loss is observed. We found this to be one of the most effective and valued tools to understand the cause of low yield. Over the course of time, we have correlated specific yield patterns with specific fabrication steps. These are in the category of known process sensitivities. Test results are verified to rule out a test issue. The trend data is analyzed to determine if the low yielding lot is a one of kind lot or whether a large shift in the process has occurred and many more low yielding lots are potentially on the way. Process travelers and comments are reviewed. Commonality studies are performed. Bench measurements are made. If warranted, FIB cross section and SEM/TEM are performed. When a root cause is found, it is added to our list of known issues. The result of the analysis is fed back to the Process Engineering group. Corrective action is taken to prevent future occurrences.

TYPES OF YIELD LOSS

Skyworks tracks the end to end yield by wafer fab and product. The wafer fab end to end yield is simply how many die you ship divided by how many die you started into the fab. The causes of yield loss fall into several broad

categories. These are design, wafer fab, and test. These in turn can be further broken out as follows:

- Design yield loss:
  - Design topology
  - Device model accuracy
  - Design Layout rules
- Wafer Fab yield loss:
  - Wafer fab survival yield through PCM is impacted due to breakage, equipment failures, misprocessing, process robustness, etc.
  - Process control
  - Process defects
  - Process technology/performance
- Test yield loss:
  - Wafer probe, package test, and module test
  - Gage accuracy, precision, repeatability, and reproducibility

SEPARATING THE CAUSES OF PROBE YIELD LOSS

There is a simple technique to understand probe yield losses and what limits yield. The test program needs to report functional and performance driven yield loss. A die that passes an easy functional test is operational and free of time zero defects that would cause open and short circuits. It could still have a reliability defect, but that is beyond the scope of this paper. The die functions, but the performance limits are wide open. An easy functional failure is generally related to some type of wafer fab defect mechanism. Conversely, a die that passes a performance test meets the full RF spec limits over all required test conditions. Performance test failures are more complicated and can be due to design, process control, or process technology capability.

When the yield of multiple products with different die sizes in the same process technology is available, the defect density of the wafer fab can be obtained by utilizing a yield model. There are many published yield models in the literature. A simple exponential model is a good place to start. Yield = $e^{(-d0 * Area)}$, where d_0 is the defect density and area is the chip area. When the yield versus area is plotted, a pattern will likely emerge. An exponential fit will reveal the defect density. It is easy to see if most of the products fall on the line or not. Products that fall close to the line exhibit common cause variation. Products that don't fit close to the line have special cause variation.

The improvement of defect density is addressed by working within the wafer fab to identify the types of defects. Automated visual inspection equipment is utilized with a process segregation technique to find the offending process steps.

Performance driven yield loss is addressed by identifying the failure mode and searching for root cause. The root cause may be process capability, product design robustness or even a test issue. Masks containing multiple versions of the same design are run. The top three failure bins are collected at wafer probe over several wafers and fab lots. Standard process splits are run. Die are characterized over temperature, voltage, and power. Design to process performance sensitivities are identified and addressed.

CASE STUDIES

The following case studies are examples of the yield improvement efforts at Skyworks Woburn fab.

CASE STUDY 1 LEAKAGE CURRENT

A weekly wafer probe yield chart showed a dip in the yield of a high volume mature product. The weekly chart review facilitated quick recognition that there was an issue impacting yield. Analysis of the failure bins revealed an increase in yield loss due to circuit leakage current. Microprobe testing on passing and failing die revealed higher gate leakage current (Figure 1). Photoemission analysis of failing devices (Figure 2) helped locate leakage sites.

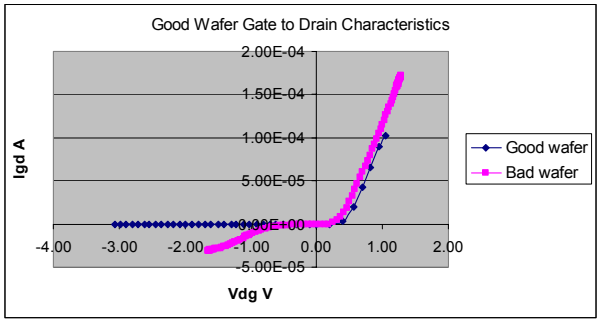

Figure 1: Bad wafer showing higher leakage than good wafer

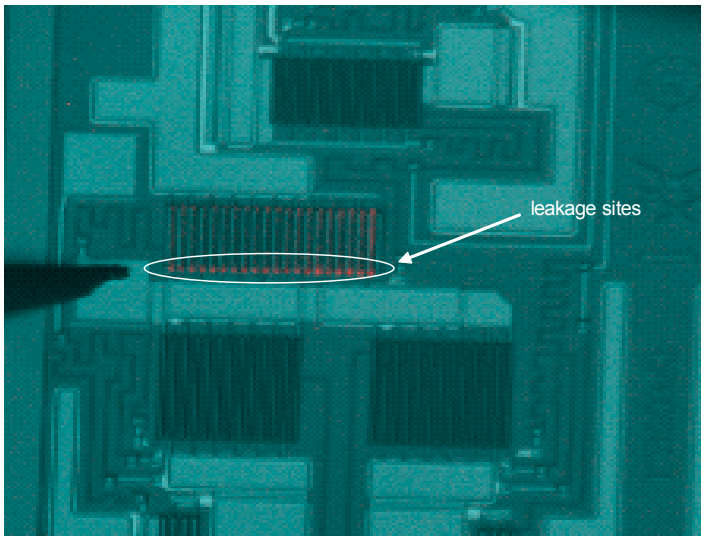

Figure 2 Photoemission imaging showed hot spots of leakage current

FIB-TEM cross sections and EDS analysis at the diffused metal location revealed gold diffusion into the GaAs substrate (Figure 3 and 4).

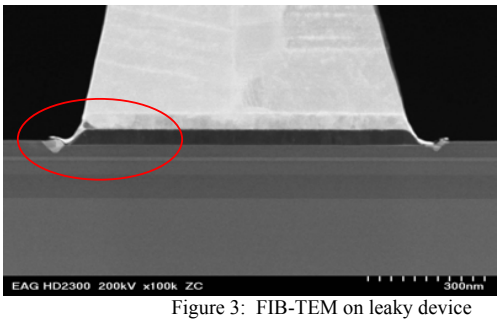

Figure 3: FIB-TEM on leaky device

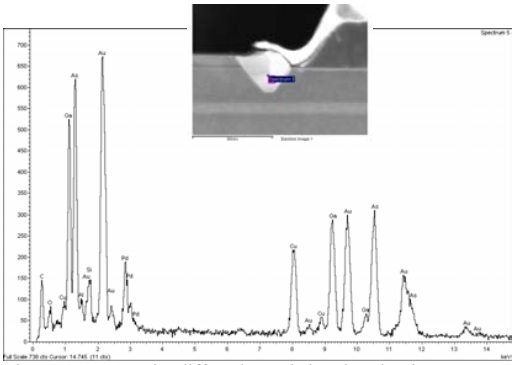
Figure 4: EDS at the diffused metal showing dominant Au peak

Process control data of the gate metal deposition process did not highlight any issues. Commonality analysis of the history of good and bad lots indicated a particular metals evaporator was linked to the vast majority of failing lots. Using this information, the equipment was thoroughly reviewed and adjustments were made. Confirmation lots were quickly run. Leakage current and probe yield returned to normal. The Yield Improvement Team had quickly recognized an issue and identified root cause within two days. This was possible because the people resource, data, data analysis software, and F/A equipment were all available to the Yield Team. Subsequently, an effort was undertaken to optimize the metal deposition process. After optimization, the wafer probe yield was increased to a record level.

CASE STUDY 2 SCRIBE CHIP OUTS

Skyworks utilizes automated visual inspection to remove defects that either do not cause electrical failures or occur after wafer probe in the wafer thinning and dicing process steps. Yield through the visual inspection process is charted and routinely reviewed. Continuous yield improvement goals are set each year for the end to end yield. This includes the outgoing visual inspection yield. The automated inspection tool has the capability to capture images of the defects it finds. These images are reviewed and categorized. A Pareto of the defects observed revealed scribe chip outs as the top yield loss category. A yield improvement effort was undertaken to understand the root cause of scribe chip outs. The investigation pointed to the tape mount process used prior to scribe. Upon break, the tape provided insufficient lateral pull to consistently separate the die. Adjacent die that did not separate quickly had the opportunity to chafe against one another resulting in a chip out. Further improvements were made to the break force and post break clean which resulted in two full percentage points of visual yield improvement.

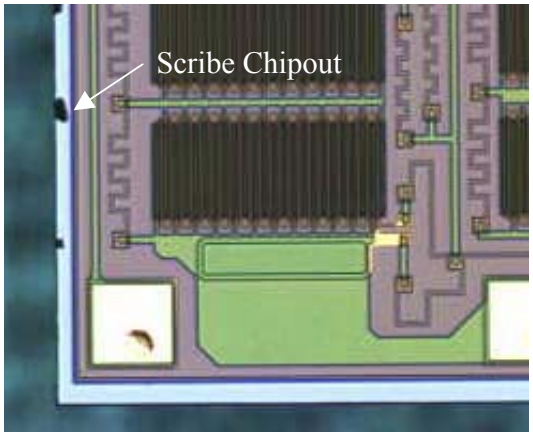

Figure 5 Picture showing scribe chip out

CASE STUDY 3 CHANNEL ETCH OPTIMIZATION

Our test engineering group developed software, known as the "Parameter Viewer", which allows us to provide a wafer map of any test parameter as well as the overall yield. The tool is web based and can be accessed from anywhere by Skyworks personnel. This tool makes patterns obvious that would be very difficult to "see" in a table of data.

As devices become denser and design rules shrink, interesting patterns can be seen. One of these patterns, we called the "PCM effect," where only the devices surrounding the PCM's were good (i.e. low leakage) (Figure 6).

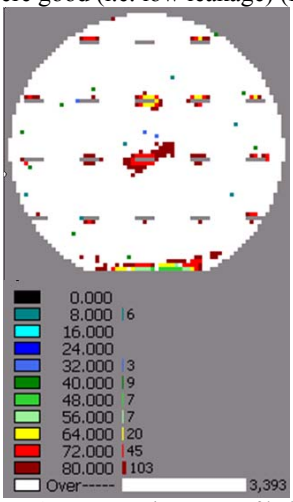

Figure 6 Parameter Viewer map of leakage current

We speculated that the etch chemistry has a localized loading effect. Our PCM areas were very lightly populated with devices and therefore etching of the test FET recesses occurred quickly. As one moves farther away from the PCM, and into the denser devices, the device recesses became underetched, requiring more etch time than those of that of the PCM. Figure 7 shows a plot of over-etch percentage required vs. amount of open area.

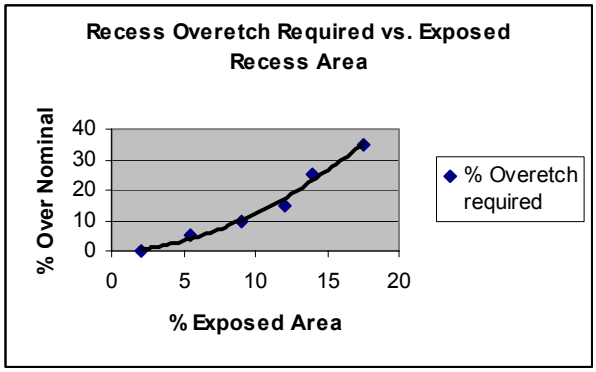

Figure 7 Required over-etch vs. exposed area.

Because of the potential for PCM-to-device mismatch as the PCM becomes over-etched, we moved to an alternative etch chemistry. The new chemistry did not exhibit a localized loading effect and the "PCM effect" was eliminated.

CASE STUDY 4 DRAINING THE YIELD SWAMP: INCREASING THE ABILITY TO DETECT SMALL YIELD LOSSES

Continuous yield improvement efforts were successfully applied to a specific high volume product. Over time, the yield of this program improved from infamously variable and unpredictable, to prominently high and stable. A subsequent minor degradation was detected. This level of yield reduction likely would have been lost in the noise of the previous process' distribution. (Figure 8).

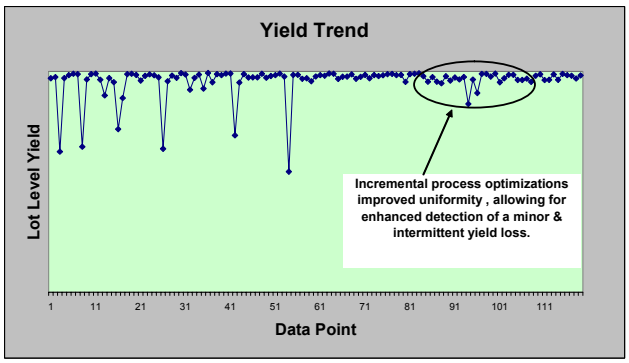

Figure 8 Yield Trend Chart showing improved yield. and tighter distribution, over time

Mapping software results, of product highlighted in Fig. 8, showed the vast majority of failing chips were relegated to the extreme outer edge of the wafer, and failed the Idss measurement (Figure 9).

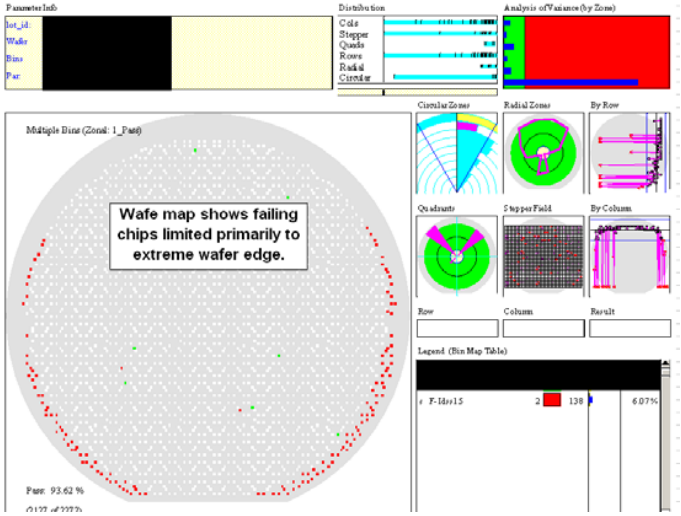

Figure 9 Example of dataPOWER® [3] Lot/wafer Report mapping/summary software.
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A commonality study suggested a lower yield for lots which included epi material from a particular vendor. Analysis of final probe results, filtered by epitaxial material vendor, statistically confirmed a difference in Yield distributions between the two vendors (Figure 10).

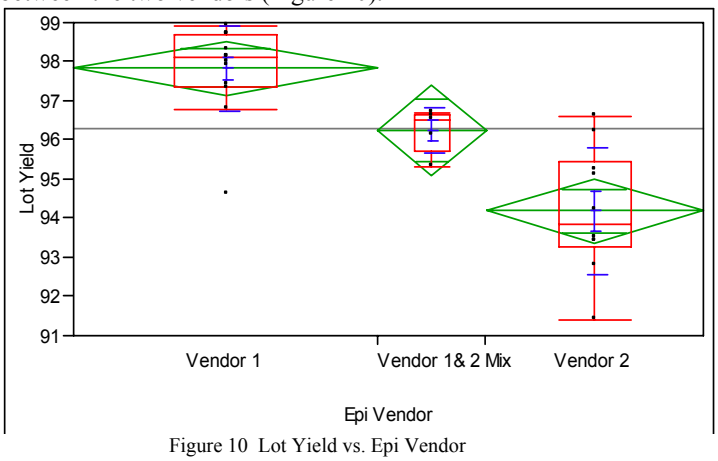


Figure 10 Lot Yield vs. Epi Vendor

Feedback was provided to the vendor in question, who is working to improve their epitaxial uniformity at the wafers' edge.

An important observation in this case study is when the yield is stable and predictable, more subtle occurrences of yield variation can be readily recognized and investigated. Earlier in the lifespan of this product a 4%, intermittent yield loss would not have been as easily highlighted. Moreover, when small, but measurable, sources of yield loss are

identified and corrected, the benefit is enjoyed by all products that use that process module which was improved. This provides a rationale argument to continue yield improvement efforts on high yielding products.

CASE STUDY 5 RF PROBE CARD OPTIMIZATION IMPROVES YIELD

Skyworks Woburn fab utilizes (*data*POWER®) software to query our database and analyze results. One feature of the software facilitates stacking the yield of multiple wafers to find die that never pass. Applying this tool revealed an interesting pattern. Every other row of die failed at the edge of the wafer. The pattern was not random. Consequently, a test issue was suspected. The investigation led to probe card design. A probe card with improved isolation and RF matching eliminated the yield loss. The measured isolation improved by 4 dB.

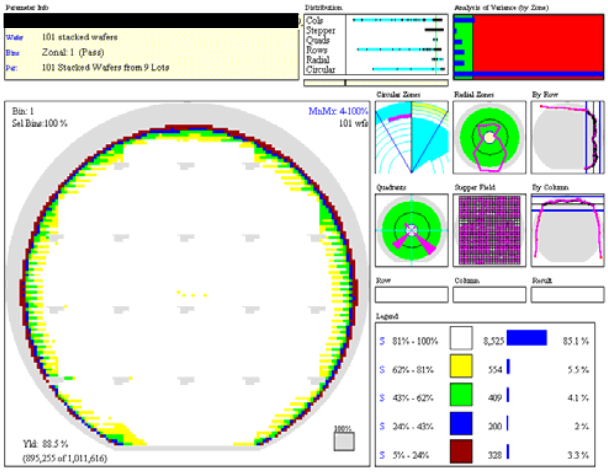


Figure 11 *data*POWER® stacked wafer yield map showing yield loss due to probe card

CASE STUDY 6 Idss UNIFORMITY

Many of the problems we've encountered involve unexpected loss of Idss. Figure 12 is an example of a problem Idss wafer showing severe edge loss.

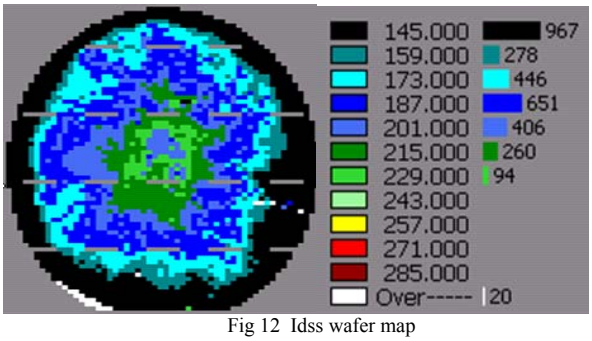


Fig 12 Idss wafer map

Since the pass/fail pattern was ragged we suspected a process problem and not an epi uniformity issue. Fig 13 shows a FIB-TEM of the FET's from the bad area.

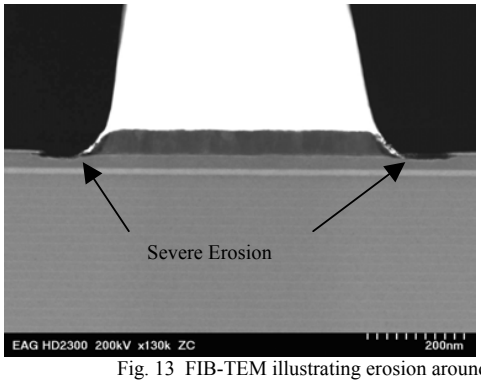


Fig. 13 FIB-TEM illustrating erosion around gate

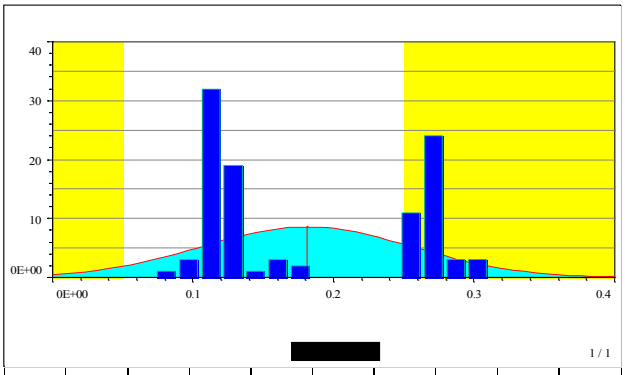
What we found was severe erosion of the GaAs material in the vicinity of the schottky gate. This effect has been well documented and has been referred to as galvanic corrosion or electro-chemical etching [2]. It can occur around ohmic metal as well as gate. When we presented this information to Process Engineering, focus was quickly directed to a particular piece of equipment, which was confirmed to have water contamination in the stripper chemistry.

CASE STUDY 7 LOW CURRENT DENSITY

Having the appropriate analytical and operations tools readily available to a yield team is critical to ensuring an expeditious resolution to a given problem. The following case illustrates how having the right tools on hand (or in this case on a laptop) helped to quickly focus an investigative effort in the correct direction.

In this case study, lower than normal current density was noted during in-process checks of a small number of specific lots. A related PCM (Process Control Monitor) was shown to correlate with the current issue. Engineering Team meetings were convened to discuss the problem. At Skyworks-Woburn, a Process Engineering meeting typically includes the engineers responsible for each key area of the fab, Yield Engineering representatives, Integration Engineering, Quality Engineering, and Operations representatives. This provides a wide diversity of expertise, and ensures a multi-disciplined thought process, critical to maximizing the potential of the investigative team.

The meetings commenced with a discussion of the issue at hand. Lots were identified and brainstorming began. During the course of the brainstorming discussion, *data*POWER®, a data gathering, stats/analysis software package employed at Skyworks, was actively being used to quickly look at the PCM results of highlighted production lots. One of the subject lots clearly showed a bimodal distribution within the lots total distribution. (Figure 14)



Group	Count	Lower limit	Upper limit	Mean	Std dev	Q2	Cpk	Cp	Actual yield loss
3437179.S	102	0.050	0.250	0.181	0.075	0.127	0.307	0.445	0.392

Figure 14. *data*POWER® histogram showing bimodal results w/in the lot.
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Drilling down deeper using *data*POWER®, it was quickly apparent that the performance variation was grouped by wafer, within the lot. (Figure 15)

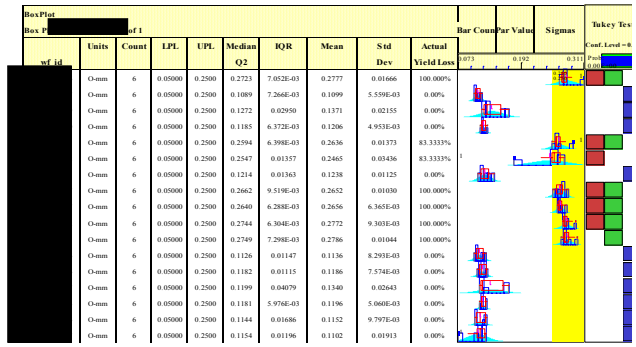

Figure 15 *data*POWER® box-plot analysis of parametric results grouped by wafers, w/ Tukey test
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Skyworks is a paperless fab so the process traveler for this lot was quickly brought online. A review of the lots' electronic history indicated a photo rework at a stage that logically would have a relationship to the parameter-in-question's performance. It was also noted that the rework was performed on only a portion of the lot. Comparing the rework list with the box-plot wafer level performance analysis, we quickly confirmed those wafers which were reworked corresponded to the "good" group. From this information, we knew which area of the process to concentrate our efforts upon. A theory was formed and quickly confirmed through subsequent experimentation.

In summary, because the investigating team had access to real time data retrieval & analysis tools, process control information, process lot history, and CAD layout viewing tools, the Team was able to brainstorm, while simultaneously analyzing data to confirm or reject key ideas. This enabled the Team to quickly form a hypothesis and generate an action/response plan, all in the span a few brief meetings.

CASE STUDY 8 MBE MATERIAL AND FAB PROCESS INTERACTION

In this case study, what initially appeared to be an intermittent yield signal, was found to be the result of an interaction between materials and etch tool. Wafers were grown from two different MBE reactors, and processed through two recess etch tools. Control leakage was very low for material from both reactors in one etch tool, but for the 2nd etch tool, only one of the reactor groups performed well. The 1st etch tool showing very low control leakage is a single wafer process tool for recess etch while the 2nd etch tool showing high circuit leakage is a batch process tool.

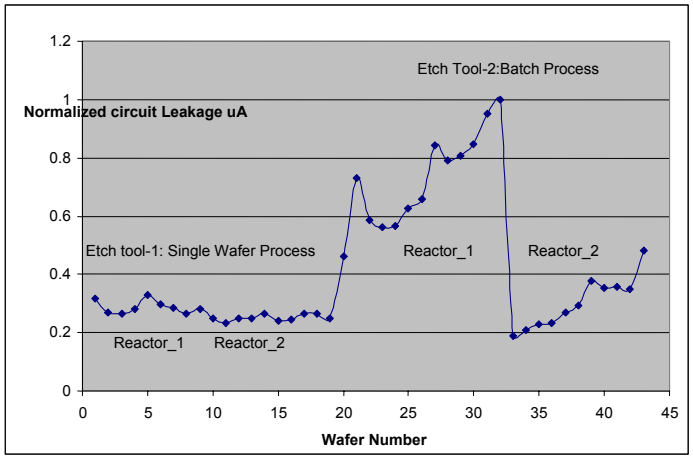

Figure 16: Circuit leakage affected by MBE reactors and etch tools.

CASE STUDY 9 INVALID WAFER TEST PATTERNS

Yield loss can occur due to invalid test results. With the help of the Parameter Viewer, some commonly occurring test patterns for various test parameters were identified. Figure 17 shows the yield loss occurring due to questionable insertion loss, isolation, and 3rd harmonics. When examples such as these were identified in production, the Test Engineering Team is alerted and addresses the issue.

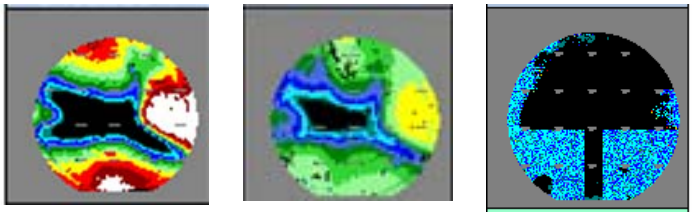

Figure 17: Examples of invalid Insertion Loss, Isolation, & 3rd harmonic tests. Failing sites are black

CONCLUSION

This paper presented the successful yield improvement strategy used by the Skyworks Solutions GaAs pHEMT Switch Fab. This strategy employs an engineering team, software, and analytical equipment to investigate and increase yield. Elements of this approach were discussed, including skills of the team, tools utilized, and improvement techniques. Several case studies were presented to illustrate the efforts and success of the Yield Improvement Team.

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[3] *data*POWER® from PDF Solutions, Inc

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ACRONYMS

pHEMT: Pseudomorphic High Electron Mobility Transistor
IMD: Intermodulation Distortion
PCM: Process control monitor
YIM: Yield impact metric
F/A: Failure analysis
PSA: Product Sensitivity Analysis (*data*POWER® application)