Discovery and Elimination of Defects Causing Yield Loss on E-FET Power Amps

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Abstract

A defect was found that was causing gate leakage resulting in product failure. The defect caused oxide to remain underneath the gate metal which prevented the device from turning off completely. The defect was traced to the photolithography portion of the E-FET gate definition. Experiments showed that the defect was not caused by a drying tool as suspected, but by a rinsing tool. The defect was eliminated by removing the dump and spray part of the rinse process and changing to a cascade-only rinse process.

INTRODUCTION

A 10 mm E-FET power amplifier is a critical component in a new TriQuint product. To minimize power drain, off-state leakage must be kept to a minimum. Any defect that causes the device to not shut off completely can ruin the IC, and, with such a large FET, there is plenty of area to accumulate defects. During product development it was discovered that the product suffered significant yield loss (up to 20%) from a new fab defect causing failures for high leakage currents.

We had to determine what was causing the defects that were not being seen in normal microscope inspection and were only being caught by diesort testing. Once we were able to "see" what the defects were, we had to come up with process alterations to eliminate them. As this product was on a tight schedule, the defect cause and a solution to the failure had to be determined in 2 months. There was only time to process two experimental lots all the way to test, so experiments had to be directed and meaningful.

SCREENING FOR DEFECTS

A die level test was developed and used to look for leakage on the 10 mm E-FET. On a good die, this parameter would typically be 4-5 uA when the FET was off. Some die were found to have upwards of 50 or 100 uA of leakage, indicating a failure of the gate to properly shut off the device. This test would be used later to evaluate our experiments.

DISCOVERY OF THE DEFECTS

Initial work on the mechanism of the gate leakage was performed by our Failure Analysis group. They did a wonderful job of "looking" at a leaky part and discovering the defect that caused the leakage. This work gave us a clue as to where the defect could be originating.

Using IV curves, our Failure Analysis group was able to track down individual leaky devices. When they examined these through an optical microscope, they were able to find defects in the gate features (Fig. 1).

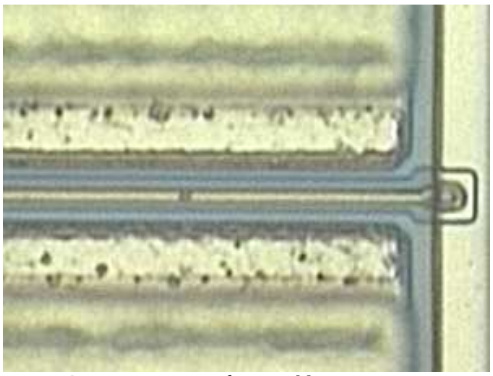

FIGURE 1: E-Fet Defect Visible in Microscope

They then obtained STEM images along the width of a gate and through one of the defects (Fig. 2).

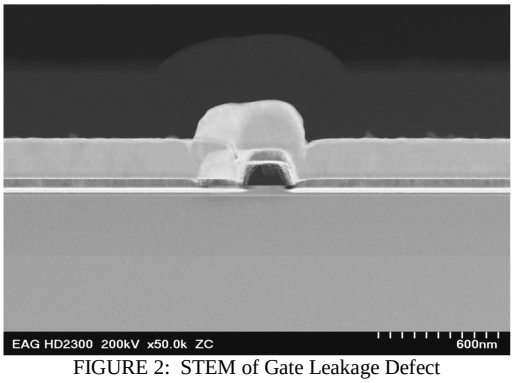

FIGURE 2: STEM of Gate Leakage Defect

EDX was performed on the defect and the surrounding areas. The cause of the gate leakage was clearly found to be SiO2 between the channel and the gate metal preventing the gate from shutting off in that area (Fig. 3).

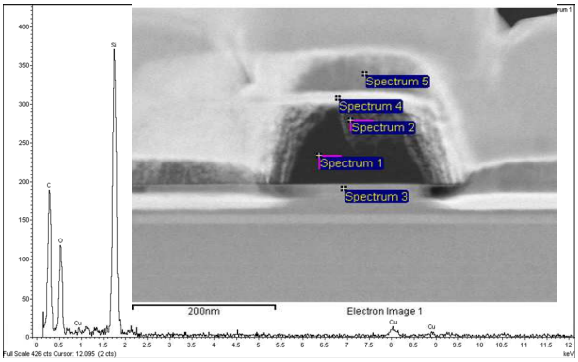

FIGURE 3: EDX Shows Defect is SiO2

As SiO2 is the dielectric that we etch through to make gate contacts, we believe that a particle was blocking the etch. We believe this particle was then being removed by wet treatments in subsequent steps since, to date, the particle itself has never been found. It was always gone by the time analysis was done on the gate, and the only thing left behind was un-etched SiO2.

CLUES TO DEFECT ORIGIN

The first clue, obviously, was the remaining SiO2. This told us to look at the steps prior to Gate Oxide etch. Another important clue was that the defects were often clustered together, near the center of the wafer, and they rotated around the center in a random pattern. Thus the failure was termed a "paddle" defect which led us to suspect that a specific tool with a paddle wafer loader was the cause (Fig. 4).

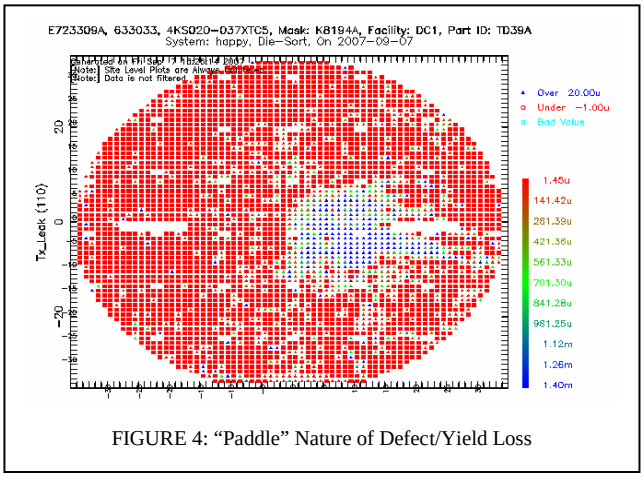

FIGURE 4: "Paddle" Nature of Defect/Yield Loss

The rotation of the "paddle" signature also indicated that the wafers were not aligned in the same orientation when the defect occurred. In the end though, the most important clue was a simple first wafer effect. On all lots of this product, one wafer always yielded up to 15% better than the rest of the lot with no cluster of leaky sites, presumably, we thought, because it never had a paddle over it. This wafer was what we wanted all wafers to look like.

A team member noted that the defects looked similar to some "scumming" defects that we had seen months earlier. These "scumming" defects were eventually traced to a faulty drier. This observation directed us to the process area where we found the defect, though in the end, it is not believed that the "scumming" defect seen earlier was related to this defect.

EXPERIMENTS

Our first experiment was to determine wafer order on 2 lots as they ran through all sections of the E-FET construction process. We would not receive test data until weeks later so we proceeded with a "screening" experiment while we waited for these results.

Our "screening" experiment examined multiple causes of the defects that had been brainstormed by our team. We tested for un-lifted metal from previous processes, the failure of the suspected dryer (both by forcing the dryer failure and by skipping the dryer), alternate E-FET oxide etch processes and methods to etch away the defect. An alternate rinse and dry process was created which allowed us to skip both a sink and a dryer. Wafer order was recorded as well.

Results for both experiments came at the same time and both pointed to the step in the process immediately after the E-FET PR develop but before the E-FET oxide etch. There is a rinse and dry process in between these steps. The ordering experiment pointed to the wafer in slot 25 during this process step as having the highest yield. The "screening" experiment showed that any wafer without a wafer back facing it during this process step had much higher yield. Furthermore, the wafers that received the alternate rinse and dry process had higher yields regardless of their order. The theory of a failing dryer seemed to be supported.

Our follow up experiment focused on this rinse and dry process to determine which of the two was responsible. An alternate drying tool was utilized that also offered a rinsing option. Rinse processes were developed within both of our dryers. The alternate rinse and dry process was used again to eliminate a dryer altogether. Wafer orientation was recorded as well as wafer order as a further guide to determining the defect's source.

The surprising results from this experiment (Table 1) showed that the rinse process and not the dry process was causing the defects. Using the wafer orientation experiment, we were able to determine which region of the wafer was exposed the longest to air during the rinse process. The defects were always on the region of the wafer exposed the longest. When the dryer was used for both rinsing and

drying, yield improved significantly. And when an alternate dryer was used with the control rinsing process, yield was lower.

TABLE 1
RINSE AND DRY EXPERIMENT RESULTS

Rinse	Dry	DS Yield %	Comments
Std	Std	84.9	
Std	New	90.0	
Std	Std	93.0	In slot #25
New	None	92.8	
None	Std	92.8	
None	New	93.3	
None	None	93.7	

We think the spraying action of the rinse tool on the backs of wafers was dislodging small GaAs particles that were landing on the face of the wafers behind them. These GaAs particles could have been created by developer attacking the GaAs surface on the back of the wafer, thus allowing a strong water spray to dislodge them. The rinse process involved dumping the water and using a water spray to keep it wet while the wafer was exposed to air.

We then considered that perhaps it was not necessary to dump the water. The volume of developer rinsed off was small, so it was diluted as soon as the wafer was submerged in water making further dilution through dump rinsing unnecessary.

Immediate action was taken to remove this spraying action from the post-develop rinse process. The process was changed to incorporate a cascading rinse action with no exposure of the wafer to air or water spraying. This seems a simple solution to such a critical problem, but it could not have been anticipated earlier given the presumed benign nature of a water rinse. The process improvement was instituted one week ahead of the 2 month deadline. Follow up lots showed yield improving from ~83% to 93-96% for the die level leakage test (Fig. 5).

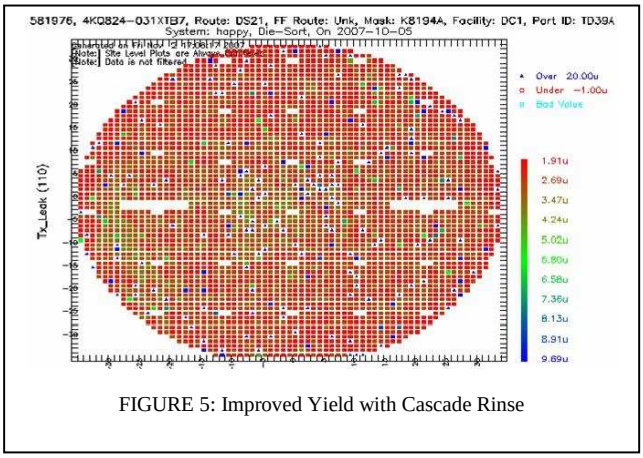

FIGURE 5: Improved Yield with Cascade Rinse

CONCLUSION

A defect-related failure caused significant yield loss to an important TriQuint product. Under a tight product development schedule, this defect had to be eliminated quickly. A focused team was brought together that brainstormed and tried possible solutions.

A combination of communication, process understanding, and strong failure analysis work directed us to the photo process defining the E-FET gate. We found that the rinse process prior to the dry was the cause. The rinse process only needed elimination of a spraying process to remove the defect. Product yields improved as much as 20%.

Another lesson learned from this problem is the role assumptions can play when searching for process abnormalities. The labeling of the defect as a "paddle" defect caused us to narrowly focus on tools with robot arms and paddles early on. This caused us to focus efforts in the wrong direction. When the defect was noted to be similar to a previously-solved "scumming" problem, we were led to the correct sequence in the process, even though a different tool was involved for this issue. Again it was important to not focus too intently on the tool we assumed was the cause. In fighting process defects, assumptions can and are made, but they should not be blindly followed and must be scrutinized repeatedly to avoid moving too far in the wrong direction and losing valuable time.

ACKNOWLEDGEMENTS

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ACRONYMS

E-FET: Enhancement Mode Field Effect Transistor
EDX: Energy Dispersive X-Ray Analysis
STEM: Scanning Transmission Electron Microscopy