

## Defectivity Yield Improvement Activity to eliminate nitride blisters

Mike Clausen, Jason McMonagle, Bela Green, Gayle Murdoch, Andrew Miller, John Cullen, Jim Moran

Filtronic Compound Semiconductors, UK Tel. +44 1325 306013

email: [mike.clausen@fics.com](mailto:mike.clausen@fics.com)

**Keywords:** Via, Blister, MMIC, DMAIC, Six Sigma

### Abstract

The manufacture of GaAs MMIC devices typically requires the use of via technology to provide both a heat sink for temperature control and a low inductance ground for improved electrical performance. Filtronic Compound Semiconductors design and manufacture a comprehensive range of MMIC device within their product portfolio. Following completion of the manufacture process, an end of fab visual inspection is carried out to assess defectivity levels in order to guarantee quality of product to the customer.

During a standard end of fab visual inspection, a defect was observed in the form of lifting/blistering of the nitride layers in the vicinity of via pads. This paper reviews how Filtronic Compound Semiconductors instigated a project initiative to analyze the extent of the problem, implement containment activities, introduce countermeasures and control the resultant reduction in defect levels through six sigma methodologies [1]

### INTRODUCTION

Filtronic Compound Semiconductors manufacture a range of MMIC devices for a broad range of both commercial and military applications. These devices are manufactured on a number of process routes that utilize both generic process modules and dedicated process modules depending on the specific application. Following the manufacturing process, it is customary to inspect fabricated die to assess defectivity levels prior to DC/RF PCM wafer acceptance testing.

During a standard visual inspection carried out on a particular product type, a defect identified as a nitride blister was observed. The defect took the form of an area of lifting nitride in the vicinity of the source pad. An in depth inspection of a range of product applications within the fabrication area indicated that the defect was restricted to certain process routes only. The defect was random in its appearance and the levels were such that up to 30-40% of the wafer could be affected at any one time and in extreme cases this would result in wafer scrap, a costly exercise having completed the fabrication cycle. Although the defect did not appear to have any noticeable impact on the electrical performance of the device, there was an obvious concern on the reliability performance. In order to ascertain the impact of the defect from a reliability perspective, reliability testing on affected parts was undertaken in the form of temperature reflows under a range of typical package conditions. It was observed that formation of the defect was accelerated under

these conditions. In addition to the obvious concerns over device reliability that this defect presented, there was a significant impact on cycle time necessitated by the increased visual inspection and subsequent disposition of affected product lots at the end of line. Due to the high customer demand for this product type, this issue presented a significant impact commercially on this business critical device and as a consequence senior management instructed the formation of a cross-functional project team to provide a structured solution to the issue.

The scope of the project team was to identify the cause of the nitride blistering, instigate appropriate containment activities, implement suitable countermeasures and to control and monitor the improvement processes.

### PROCESS INVESTIGATION

The approach taken to investigate the problem utilized the established "six sigma" DMAIC methodology. This methodology sets out the five steps that form the basic framework of problem investigation [2] namely:

**DEFINE** – the problem is defined, its impact to product and quality, affected stakeholders, resource, timelines

**MEASURE** – the key process metrics are identified and baseline data is collected relating to the project goals and targeted customers.

**ANALYSE** – the data collected from the measure stage is analyzed and theories identified to explain potential root causes.

**IMPROVE** – the potential solutions are identified, prioritized, risk assessments performed and corrective actions are implemented.

**CONTROL** – the process solutions are implemented with effective process controls, training and monitoring.

The first stage of any planned project activity is the careful formation of a cross functional team that encompasses personnel from a number of key disciplines. This provides a broad range of skill sets that collectively cover a range of disciplines. The project team selected drew on resource from process, equipment, yield and product engineering to provide a breadth of experience.

A “champion” for the project was elected from senior management to report progress at board level and to act as an interface for negotiating any resource and budgetary requirements. The first stage of the activity dealt with defining the project charter. This covered the problem statement, business impact, goals, resource and associated timelines. Figure 1 shows a typical blister defect associated with a source pad as identified during the standard end of fab visual inspections. The defect takes the form of lifting / blistered nitride in the vicinity of the pad

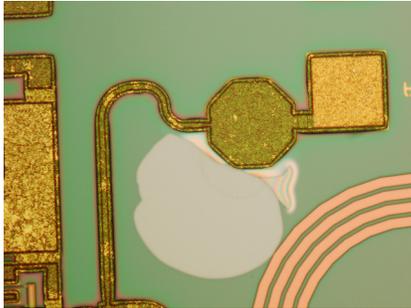


Figure 1: Typical nitride blister defect picked up during end of fab visual inspection

As can be seen the defect identified took the form of lifting or blistered nitride around the via pad of the device. A typical MMIC device would utilize up to 4 nitride layers during its construction, and in this instance, the lifting nitride would be a combination of all layers from the GaAs surface. An initial assessment of a number of product lots for different applications indicated the following:

- Only certain product routes were affected
- Random numbers of wafers were affected in lot
- 0% - up to 35% typical defect level
- Defects were typically clustered at wafer edge

During the initial stages of the problem occurrence it was paramount that an effective containment activity was implemented to ensure the quality of devices shipped to customers. A rigorous visual inspection activity was implemented with criteria applied. This was performed by dedicated inspection processors as part of the standard visual inspection criteria. Inspectors would fill in a wafer map at a shot level to indicate severity and type of defect. For lots exhibiting above an agreed % of affected shots, an LTR (lot trouble report) would be raised on MES (manufacturing execution system) Images would be taken by the on shift process technicians and stored on a common network to provide a portfolio of evidence of the defect type and magnitude. In order to disposition the affected wafers, affected and non affected die would be subjected to extensive reflow analysis in addition to the standard DC/RF PCM electrical WAT data. The results would be reviewed before a select committee to screen out affected areas of the wafer to

enable die shipment. This provided an efficient containment of the problem during the initial investigative process.

The project team concentrated on setting up a stringent investigative process to ascertain the extent of the problem and to gather data on defect type and defect location.

During the initial stages, the team agreed that all affected production lots be held for detailed inspection by engineering personnel at the end of the fabrication process. This allowed a portfolio of blister defects to be produced which could be utilized to educate and train production personnel in the various modes observed. This activity ran for 4 weeks during which a number of product lots were identified, and a portfolio of typical defects were logged, photographed and recorded on a database. Following this, dedicated teams of inspection processors were assigned within each production shift to perform detailed inspection of product device wafers over a 4 week period at various stages through the production cycle over a range of process routes. The project team met on a weekly basis to review the data and ensure the containment activity was effective and satisfied quality and reliability controls. Key performance indicators were defined and all data was characterized to understand defect location on the wafer, trends within product lot, trends between different process routes and where during the fabrication cycle the onset of the blister defect occurred.

#### PROCESS RESULTS

Analysis of the inspection data indicated that the defect was typically observed to be in clustered areas, and predominantly exist around the wafer edges. Observing closely at a die level, the blister would appear to move around the vicinity of the bond pad depending on the wafer location, i.e. there appeared to be a rotational dependence. Examination of the inspection data taken through the production flow also indicated that the onset of blisters did not occur until after the formation of the through wafer via. A number of failure analysis techniques were proposed to investigate the defect. Initially, SEM microscopy was utilized to look closely at the blister area. Optical microscopy had indicated an area of staining / contamination within the vicinity of the blister (Figure 2)

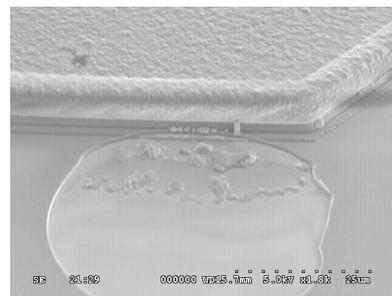


Figure 2: SEM micrograph showing contaminant within blistered area

In order to try and understand the nature of the contaminant, Auger spectroscopy was utilized. Results of the analysis indicated high levels of Potassium and Sulphur in the contaminant area. Potassium Iodide is typically used as a gold etchant during the formation of airbridges. Sulphur is used as a constituent of SF<sub>6</sub> used predominantly during the etching of non-critical nitride layers at passivation and cover layer processes. It was postulated that residues of Potassium and Sulphur may be contributing to the adhesion of subsequent metal and nitride layers during the completion of frontside and backside processing. Secondly, due to the observed rotational dependence of the defect in relation to the source pad, sections through both an affected and non-affected die were taken. (Figure 3)

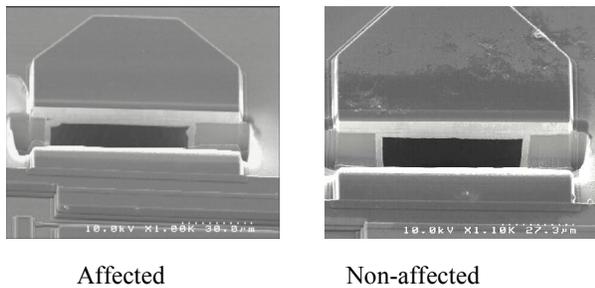


Figure 3: Images of a FIB cross-section of an affected and non-affected die

As can be seen, there is a clear correlation between the alignment of the through wafer via to the bond pad and the blister defect. A number of affected die were sectioned and presented this effect. Preparation of a sample by FIB is time consuming and only gives an indication of misalignment in either the x or y direction. An etchback process was developed to selectively remove the frontside metal and nitride layers of a product device. This would leave an imprint of the ohmic metallization with the position of the contacting via present within the ohmic layer. A clear indication of the alignment of the via was now available. In real terms, this meant that cross wafer uniformity could be easily measured. Samples could be taken from areas across the wafer and subjected to etchback to allow a clear positional dependence to be ascertained (Figure 4)

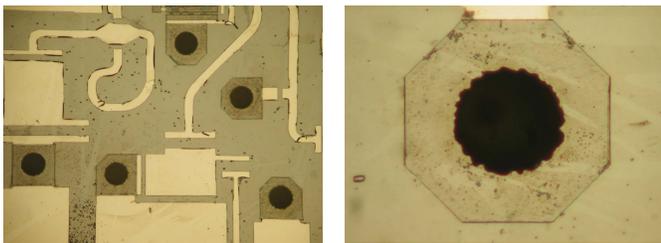


Figure 4: Devices after etchback analysis indicating via alignment

This now became a useful tool in the diagnosis of wafers evident with blisters and provided a simple technique for

monitoring via misalignment. Etchback analysis of a number of affected lots gave a clear indication that via misalignment was playing a significant contribution to the formation of the blister defect. The team concentrated its efforts on the via process, particularly via alignment. Typically, via alignment is carried out using an infrared contact alignment system. Supporting sapphires are metallized to aid clamping to the electrostatic chuck ensuring that sufficient metallization is removed to allow accurate alignment margin. Typically, two areas of metallization will be removed from the left and right hand side of the sapphire to perform accurate alignment.

In order to investigate the via alignment process, the team focused on:

- Shift Operator dependency
- Accuracy of alignment structures
- Contact Aligner hardware
- Via etch profile / CD control

Due to the manual nature of the via alignment process, there is a certain level of subjectivity with regard to accuracy of the alignment. Firstly, any operator dependency was assessed across the production shifts. A review of affected lots was cross-correlated with the MES tracking reports to check for correlation (Figure 5)

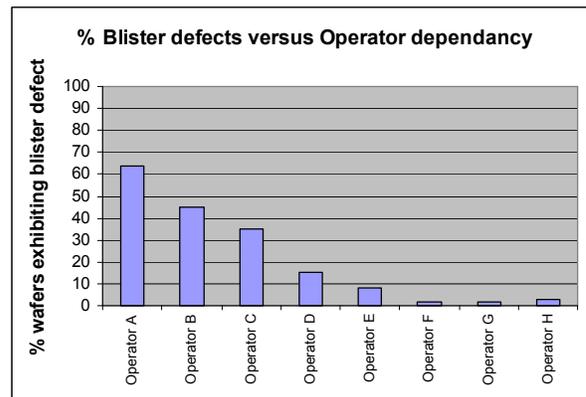


Figure 5: Blister defect versus operator alignment dependency

A clear dependency on operator alignment was observed. To address this, a review of alignment practices was performed. Borne from this, a structured training program was developed to cover all the production shifts and reassess each operator's alignment capability. Documentation and procedures were reviewed and updated to reflect the appropriate working practices. Secondly, an assessment was made of the alignment structures currently utilized on MMIC mask sets. It was agreed that a new structure should be characterized to provide a more accurate alignment process to minimize misalignment margin. Trials of this structure characterized by etchback analysis indicated a reduction in misalignment. Finally, an overhaul of the contact aligner hardware was implemented with the assistance of the vendor

who identified a shift in alignment during exposure that matched closely to the defective die in terms of cross wafer location

Finally, a process module-by-module comparison was performed to look at the specific differences between the technologies that might provide some indication as to what factors might be influencing the blister formation. A key factor identified was that the blister free process route was utilizing a new via etch process that had been developed to combat instances of pillar formation and to provide a more repeatable and clean etch profile. Due to the nature of the process development, the new improved process resulted in a final measured CD 10µM less than the standard process. It was viewed that this reduction in CD would improve any misalignment margin at the lithography stage and may be a contributing factor to the blister free performance of routes utilizing this process.

**PROCESS IMPROVEMENTS**

A comprehensive review of the visual inspection data, cross sectional, etchback and via profile analysis gave a clear indication that the position of the via aligned to the bond pad, the shape and size of the via and cleanliness of the profile was having a significant effect on influencing the onset of blister formation. In order to test these theories, process modifications were introduced to the production process controlled over a 3-month period. Process routes typically prone to the defect were chosen for initial assessment. Firstly, the new via process was introduced. Production lots were split and WAT PCM data for electrical assessment of RVia coupled with structural analysis to check for metal coverage were checked to ensure no detrimental effect was seen from the introduction. Reliability studies completed the qualification. Improved operator training and procedures for via alignment coupled with the use of a new alignment structure completed the improvement introduction. The contact aligner hardware was overhauled to maximize its alignment capability.

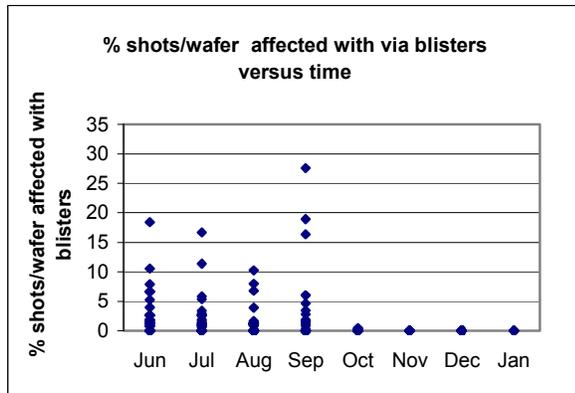


Figure 7 Blister defect levels monitored over an 8-month period

Figure 7 shows blister defect levels reported over an 8-month period. The improved process modifications reduced the levels of defective die from > 25% level on the worst affected routes to < 1% over a 6 month period. This represented a significant increase in device die available for shipment and a significant cost saving to the facility.

The final stage of the project activity was to ensure all supporting documentation was in place, that robust process control plans and data collections were implemented and that the improved performance was monitored, reviewed and communicated to the organization.

**ONGOING WORK**

The team continues to look at further optimization activities, which have been proposed during “brainstorming” sessions to improve via robustness and to provide further process latitude. These include:

- Via resist strip optimization
- Via seed metal pre-treatment and deposition characterization.
- Via gold plating characterization

**CONCLUSIONS**

Following the discovery of a nitride blister defect on a business critical product line, a cross-functional team was formed to analyze, diagnose and implement countermeasures as part of a strategic yield improvement initiative. The activity realized a reduction in defective die from >20% to < 5% over a 6 months period representing a significant cost saving to the facility. Key to the success of the project was following a defined structure using “six sigma” methodologies. Setting up a system within the fabrication area to perform visual inspections, analyzing the data, performing in depth failure analysis, implementing countermeasures and ensuring ongoing control of key performance indicators were instrumental in making the project a success.

**ACKNOWLEDGEMENTS**

The author would like to thank member of the engineering staff at Filtronic Compound Semiconductors for their dedication to this activity.

**REFERENCES**

[1] Peter S.Pande, Robert P.Neuman, Roland R. Cavanagh, *The Six Sigma Way*, McGraw-Hill, 2000  
 [2] Jens Riege, *Photoresist cuts strengthen Skyworks’ gross margin*, *Compound Semiconductor*, December 2007