Engineered Layer Transfer Substrates for Heterogeneous Integration of III-V Compound Semiconductors

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Abstract

The introduction of a mechanically weak porous layer in a III-V substrate represents a novel means by which to transfer epitaxial layers from the growth substrate. The layer may also be of a different orientation and lattice parameter than the host substrate. To efficiently remove the epitaxial layers from a host substrate, we demonstrate the fabrication of III-V template layers on porous silicon. The porous silicon is formed by anodic etching and a porous layer of a few μm is typically produced. A III-V template layer is transferred to the porous Si surface via hydrogen ion implantation and layer exfoliation. The III-V layer is smoothed by chemical mechanical polishing. The example of engineered layer transfer substrate is an InP layer on silicon. With this example, one can produce, for example, electronic or solar cell devices grown on the InP template which can be transferred from the growth substrate via the porous layer to a separate support substrate.

INTRODUCTION

Heterogeneous materials integration represents an important tool in the device performance improvement. Three-dimensional stacking of device components offers benefits in III-V manufacturing as well as in silicon technology. Recent DARPA programs, including SMART and COSMOS, are important applications of heterogeneous materials integration. In these cases, thin layers (< 20 μm) with active device components are bonded to other layers. In these cases, the transfer of a III-V device layer to another substrate requires etching or grinding away the original substrate, significantly adding to the cost and the complexity of the process.

The ability to separate the device layers from the rest of the substrate would be considered a significant advancement in this area. Separation of device layers from the host substrate has been demonstrated previously, but those methods suffer from serious shortcomings.

The CLEFT technique or "Cleavage of Lateral Epitaxial Films for Transfer"[1] exploits the lower mechanical strength of GaAs substrates in the [110] crystallographic orientation. Using photoresist, narrow trenches are defined in otherwise rarely used [110] GaAs substrates and an epitaxial GaAs film deposited by, for example, vapor phase epitaxy, which produces a continuous film by lateral overgrowth. Devices are produced over this interface and are subsequently removed by initiating cleavage through the narrow trenches and the remaining carburized photoresist. This technique has several limitations: (i) the crystalline quality of the epitaxial layer is very difficult to control by the lateral overgrowth technique; any defects present would adversely impact the performance of the device, (ii) separation of the epitaxial layers takes advantage of the fact that the (110) plane is the weakest cleavage plane, thus this technique is restricted to wafers of this crystallographic orientation, and (iii) the overgrowth material must be the same as the [110] substrate.

"Epitaxial Layer TRANsfer" or ELTRAN® is a technique for layer transfer that utilizes the mechanical properties of porous silicon to fabricate Silicon-on-Insulator (SOI) structures.[2] In this technology, a silicon seed wafer is anodic ally etched to create a porous silicon layer, which is next sintered. Next a Si layer is grown epitaxially on the porous layer, followed by oxide layer growth. This structure is then bonded and transferred to a Si handle substrate, by initiating fracture through the mechanically weak porous silicon layer, resulting in an SOI wafer. The device template layer maintains the crystallographic orientation of the porous silicon; thus, this technique is limited primarily to Si homoepitaxy.

Epitaxial Lift-Off (ELO) relies upon the high etch selectivity of AlAs compared with other materials for HF. An AlAs layer is inserted between the substrate and the device layers. Next, the device layers are covered with wax [3] or bonded to a flexible plastic substrate. However, the technique is not suitable for large scale transfer. Etch rates of AlAs are, at best on the order of mm /hr requiring long immersion times.[4] Problems with layer cracking or cleaving is known to be a significant problem with this technology.[5]

To overcome these difficulties, our approach combines a mechanically weak porous silicon layer with a III-V template layer by means of hydrogen / helium implant and layer exfoliation. The III-V template layer provides a suitable surface for epitaxial growth. After growth of the epitaxial device layers, the structure can be removed via the mechanically weak porous layer and transferred to another substrate. This concept is referred to as Cleavage fracture Engineered Layer Template or CELT.

The production of porous silicon is relatively straightforward and is well known in the literature. Anodic etching using HF-containing solutions can produce layers whose porosity varies from 10-80% and whose thickness ranges from sub-micron to several μm.[6, 7]

We have also demonstrated the transfer of a thin III-V template layer from a III-V bulk substrate or epitaxial layer to a silicon or other III-V substrate for several different III-V materials systems. The key issues here include the implantation of hydrogen – and possibly co-implanted species with a typical projected range value is on the order of 1 μm into the III-V layer of interest. Next the implanted wafer is bonded to a handle substrate. High strength bonds are achieved at low temperatures (< 200 °C) using an oxygen plasma activation scheme [8] on a silicon nitride layer deposited on the implanted and handle wafers prior to bonding, if the roughness of the initial surfaces is less than ~ 1 nm r.m.s. This annealing strengthens the interface such that the bond strength exceeds the intrinsic semiconductor strength. Higher temperature annealing (>250 °C) causes the formation of hydrogen-related platelets at the implant projected range. The temperature sequence causes the III-V layer on one side of the projected range to exfoliate from the remainder of the substrate, leaving it bonded to the handle wafer. A chemical mechanical polishing treatment is employed to smooth the surface for subsequent epitaxial deposition.[9-11]

FABRICATION

The CELT substrates combine these technologies and the fabrication process is illustrated in Figure 1:

(A) Porous silicon was produced using [001] oriented p-Si wafers in an electrolyte of HF:H_2O:ethanol :: 1:1:2 and a current density of 10 mA/cm^2 for 5 minutes.

(B) The III-V substrates are coated with silicon nitride and implanted with hydrogen. Typical implantation parameters are 130-150 keV, 5x10^{16} cm^{-2}, and cooling to -20 °C during the implant.

(C) The two wafers are exposed to a low power oxygen 'activation' plasma.

(D) The wafers are bonded together at room temperature without external pressure.

(E) The pair is annealed at ~150 °C to increase the bond strength.

(F) The pair is annealed at ~ 300 °C to produce exfoliation of the III-V layer to the bonded substrate. The ELT substrate can now be used for epitaxial deposition.

RESULTS AND DISCUSSION

The formation of porous silicon produces a layer ~ 2 μm thick under these conditions. This layer exhibits a dendritic pore structure with features on the order of a few nm as shown in Figure 1 below.

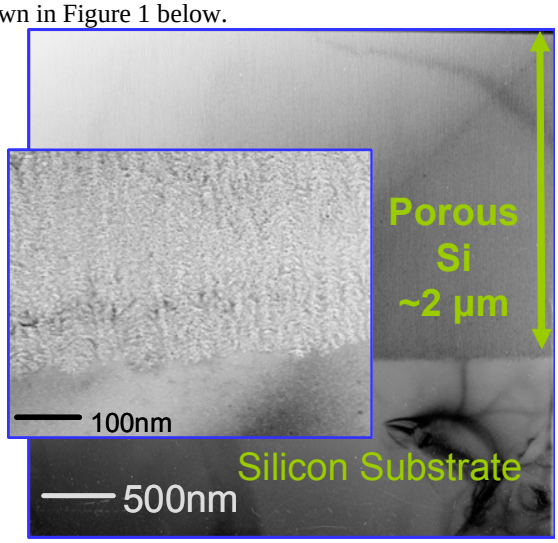

Figure 1. TEM showing formation of porous silicon layer. The dendritic nature of the porous layer is shown in the inset.

Porous silicon is known to possess lower mechanical strength than bulk silicon.[12, 13] Nanoindentation measurements confirmed that the porous layers possess a Young's modulus of about 70 GPa, which is about half the value of bulk silicon.

The surface of porous silicon can be as smooth as the initial Si substrate. This is important because wafer bonding requires flat surfaces. The AFM images below shows the low roughness of the surface after the porous silicon formation . Figure 2 shows that the surface remains smooth after subsequent silicon nitride deposition and it is suitable for wafer bonding. Figure 2(a) shows the porous Si surface and 2(b) shows the surface after nitride deposition.

After the porous silicon wafer is bonded to the III-V wafer, the wafer is annealed at 150 °C, and the interface strength increases to a value of ~ 1 J/m^2 which is on the order of the strength of the bulk wafers.

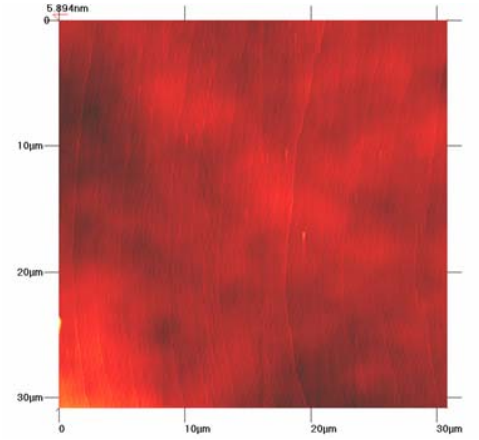

Figure 2(a). Surface of porous silicon. The r.m.s. roughness is ~ 0.5 nm.

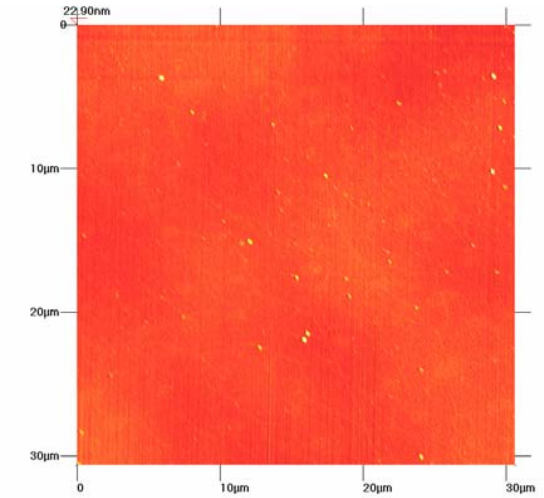

Figure 2(b). Surface of SiN-coated porous Si. ~0.5 nm r.m.s. roughness. The particulates on the surface were introduced during the AFM measurement and are easily removed during subsequent processing.

The subsequent higher temperature anneal (~ 300 °C) promotes the nucleation and growth of hydrogen platelets at the implant species projected range.[9] . Through this step, a thin layer of the III-V substrate is exfoliated from the host III-V substrate and transferred to the porous silicon substrate.

The surface of the exfoliated III-V layer is rough – on the order of the implanted hydrogen straggle – and must be polished prior to epitaxial growth. Most polishing techniques for III-V compounds remove several µm of material. The transferred layer thickness – which is on the order of 0.7 to 1.0 µm thick – would be completely removed by such a process. We have developed low removal rate polishing schemes for GaN [14], InP and other III-V compounds [15] which produce a damage-free, low roughness (< 0.5 nm r.m.s) surface for subsequent epitaxy. The TEM images in Figure 3 show an InP transferred layer surface prior to and after polishing. This surface is suitable for subsequent epitaxial growth as we have demonstrated growth of high quality InAlAs / InGaAs quantum well structures on transferred InP surfaces.[11]

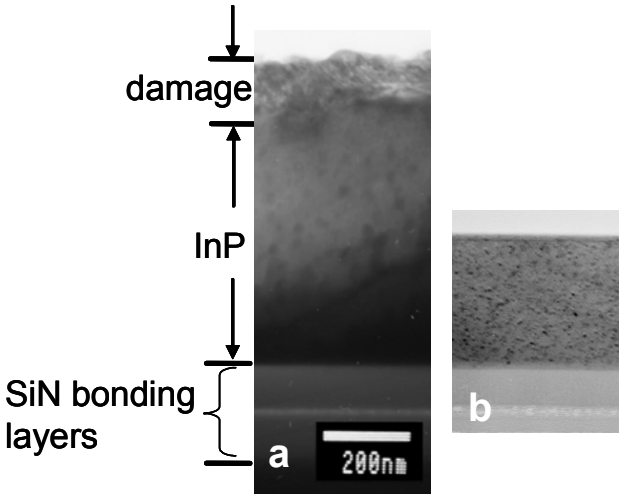

Figure 3. CMP of InP transferred layers. (a) prior to polishing, there is residual damage from the implant process. (b) after CMP, the damaged material is removed and the surface roughness is 0.5 nm r.m.s. The speckle observed in the InP layers is related to TEM sample preparation damage.

Figure 4 shows the entire structure of an InP layer transferred to porous silicon. Similar results are obtained with GaN transferred structures (and other III-V materials). The approach is modular in that the final structure is simply a series of the aforementioned independent processes. The III-V exfoliation and transfer does not depend strongly on the substrate to which the layer is transferred; the SiN-coated porous silicon substrate fabrication likewise does not require different characteristics for the different III-V layer transfer.

Another important consideration in this process is that the porous layer is sufficiently weak such that this layer is preferentially cleaved during subsequent device layer transfer. After deposition of the epitaxial device layer structure, the entire stack is bonded to a carrier substrate. This carrier substrate can be a flexible substrate, a high thermal conductivity substrate (e.g., polycrystalline AlN), or another semiconductor device structure.[16] Next, the porous structure must be sufficiently weak that any crack propagates through the porous layer and not through the device layers. It has been reported that porous silicon annealed at > 950 °C evolves to form large pores and the material weakens significantly.[17] We have developed porous surface treatments to produce significantly weakened material after annealing for a few hours at 625 °C (to roughly mimic a III-V epitaxial growth process). Figure 5 below shows an SEM image of a surface of fractured porous silicon that had been annealed at 625 °C. Large (2-50 µm) diameter pores are clearly visible at the fracture surface, which easily cleaved upon a razor blade insertion. Nanoindentation confirmed that the Young's modulus for

this material is significantly lower than the porous silicon prior to annealing.

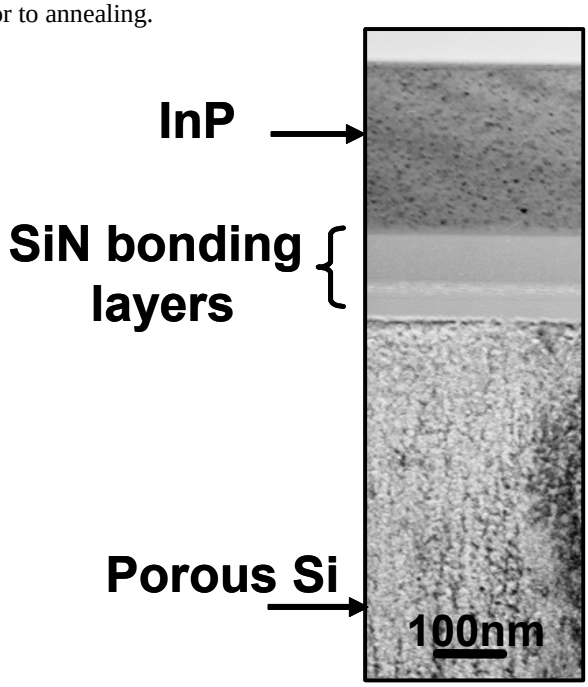

Figure 4. TEM of CELT substrate with InP template layer, silicon nitride bonding layers, and a porous silicon substrate.

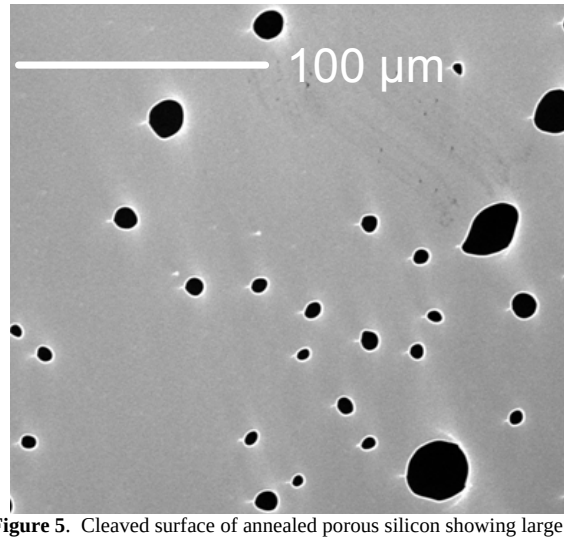

Figure 5. Cleaved surface of annealed porous silicon showing large pores that controllably weaken the material to produce a facile fracture interface.

CONCLUSIONS

Engineered layer transfer substrates have been demonstrated. These substrates employ a porous layer upon which a III-V growth template layer is transferred. The template layer is not dependent on the porous layer composition or orientation, providing great flexibility is producing device heterostructures that are independent of the bulk substrate. The mechanical properties of the porous layer promote layer transfer after epitaxial growth. This technology has applications in layer transfer, for example, for high speed electronic devices as well as solar cell heterostructures.

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ACRONYMS

HF: Hydro-Fluoric (Acid)
AFM: Atomic Force Microscopy
CMP: Chemo-Mechanical Polishing
SEM: Scanning Electron Microscopy
TEM: Transmission Electron Microscopy
CELT: Cleavage fracture Engineered Layer Template