Advances in Large Diameter GaN on Diamond Substrates

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Abstract

The use of diamond or silicon on diamond (SOD) as a thermal heat spreader substrate for GaN high power transistor and solid state lighting devices has been demonstrated previously with active devices on a small scale but not at wafer sizes of 50 to 100 mm. The capability to reduce heat has been demonstrated but the benefits of this for large volume applications such as Wimax or commercial lighting require that the technology be scaled to much larger wafer sizes. This paper will highlight recent advances in scaling GaN on SOD wafers to 100 mm diameters and will report on the electrical characterization of GaN HEMT devices fabricated on 100 mm SOD wafers. Results will include whole wafer parametric data which illustrate the large area viability and consistency of the process as well as physical characterization showing the consistency of the structure across the wafer. In addition, it will discuss yield issues related to these larger diameter substrates including film stress, wafer thinning, and packaging.

INTRODUCTION

Today's compound semiconductor industry is one of the few semiconductor industries that recognizes the value of good thermal management in RF power devices, high luminance LED's and laser diodes. High thermal conductivity packages, heat spreading sub mounts and other techniques have been in use for many years. More recently technologies using thinner die and higher thermal conductivity substrates have been implemented as chip power is pushed to higher and higher limits. Silicon carbide is now a common substrate for GaN RF devices and diamond which is the ultimate in high thermal conductivity substrates has also been used as a GaN substrate in small sizes [1] [2].

To date however, no one has reported fabrication of GaN HEMT devices on diamond based substrates larger than two inch diameter. Nor has anyone demonstrated that devices can be made with reasonable yield over large areas. Issues of the cost of thick diamond substrates and flatness of thinner diamond substrates have limited existing work to relatively small sizes but the use of SOD (silicon on diamond) substrates with GaN epi layers has largely circumvented this limitation. SOD substrates can now being made in 100 mm diameters and can be potentially be scaled to sizes up to 300 mm diameters. GaN epilayers have been successfully deposited on these substrates and active devices have now been fabricated which show the viability of the technology as well as the potential for reasonable production yields over large areas.

DISCUSSION

100 mm SOD substrates were fabricated using hot filament diamond deposition on high resistivity float zone silicon wafers and subsequently flipping and grinding the original substrate to create a thin silicon seed layer for the GaN epi layer. MOCVD technology was then used to grow the buffer, GaN and AlGaN device layers. Two different GaN layers were grown to investigate the effect on device performance as well as structural characteristics of the wafer. GaN devices layers were shown to be of sufficient quality to make HEMT transistors as reported in previous work [2].

Subsequent to GaN growth, devices were fabricated at AFRL using their standard mask set and process for HEMT devices. Prior to fabrication it was decided to cut one wafer down to 50 mm diameter to allow making a smaller gate length device. Devices were then fabricated on both wafers and electrically tested in whole wafer format with the handle wafer attached. The handle wafer was then removed from one wafer and that wafer will be mounted on a copper heat sink to allow testing of thermal performance.

RESULTS

Both wafers were processed without significant problems and yielded functional HEMT devices. Figure 1 shows the finished 100 mm wafer which has a 3x4 inch functional area as a result of a polishing defect in the silicon layer.

Figure 1
100 mm GaN on SOD Wafer

Figure 2 shows the finished cut down 50 mm wafer. The primary device which was characterized on these wafers consisted of a 2 gate transistor with 0.35 micron gate lengths and 150 micron gate width. This is shown in Figure 3 and Figure 4 which is a cross section showing the 0.35 micron gate length.

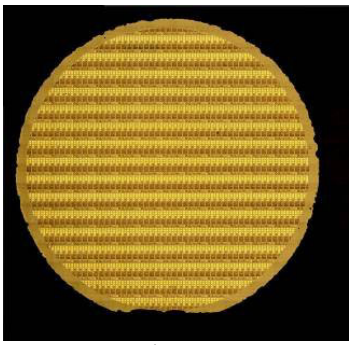

Figure 2
50 mm GaN on SOD Wafer

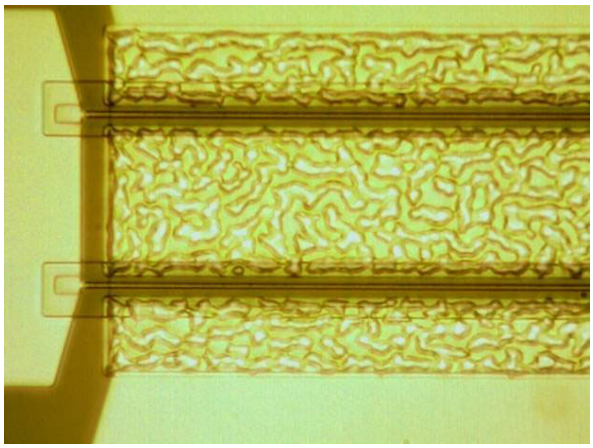

Figure 3
Portion of tested HEMT device

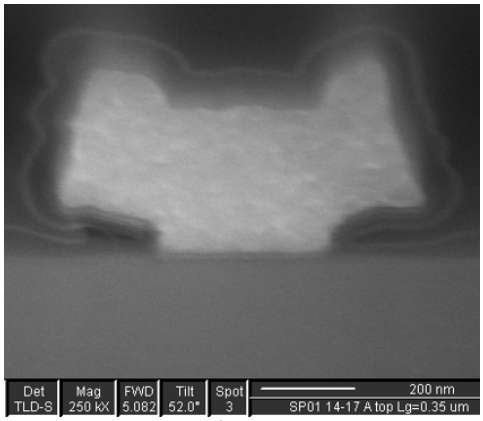

Figure 4
Cross Section of 0.35 micron transistor

Approximately 160 of these devices were electrically characterized in the functional area of the first wafer and a slightly smaller sample on the second wafer. Table 1 is a summary of the average results of that characterization. The data shows that functional devices can be made on these wafers and that the basic parameters are consistent with the geometry of the device and the characteristics of the GaN epi layer. The more important question however is whether or not this can be duplicated across the whole wafer and on more than one wafer. To answer that question requires examination of the distribution of the parametric data both statistically as well as spatially on the wafer.

Table 1
Summary of Wafer Test Results

Parameter	Wafer 1 Passivated	Wafer 2 Passivated
gmp (mS/mm)	213	223
IDS,max (mA/mm)	644	512
IGL (mA/mm)	-7.0x10-5	-2.6x10-6
fT@Gmp (GHz)	24.9	31.4
fMAX (MAG) @Gmp (GHz)	45.8	44
Device VBR (V)	50	47
Vth (V)	-1.35	-1.0

Figures 5 through 11 show the wafer maps and statistical distributions for selected device electrical parameters. Verification of the general quality of the GaN layer can be achieved by looking at the breakdown voltage of the devices on wafer 1(Figure 5). The maximum tested value was 50 volts for this parameter and virtually all devices had values above this level regardless of position on the wafer. The low level and random distribution of bad devices indicates that there are minimal fundamental structural problems with the GaN epi layer. This is supported by the gate leakage data for wafer 1 shown in Figure 6 where the distribution of high leakage devices is again fairly random although some clustering does exist toward the edges of the tested area. Figure 7 is the distribution of gate leakage currents for the second wafer which shows a similar pattern but not as high a yield.

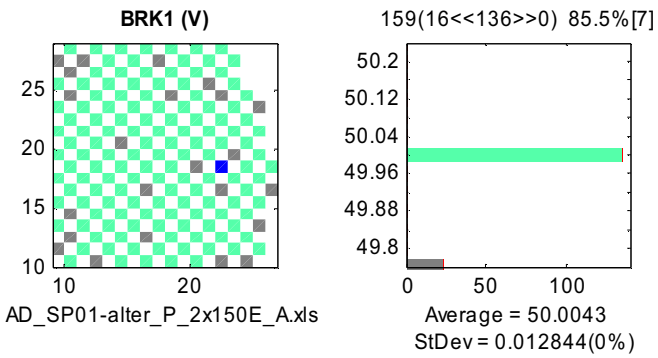

Figure 5
Breakdown voltage – wafer 1

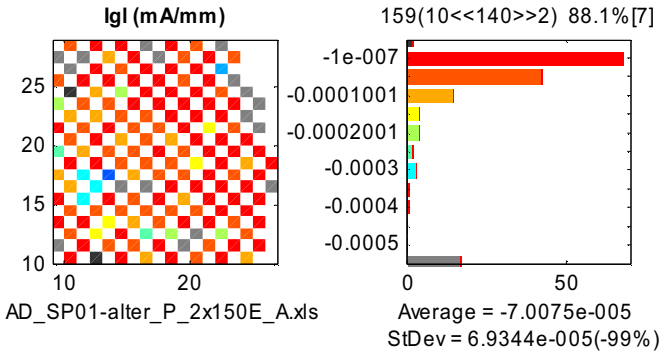

Figure 6
Gate Leakage Current – wafer 1

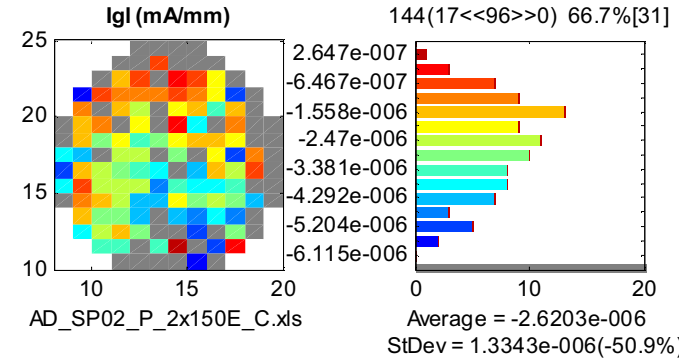

Figure 7
Gate Leakage Current – wafer 2

Given the consistency of the most basic parameters it is now practical to examine the actual device performance characteristics. Figure 8 shows the transconductance values of devices on wafer 1 which are well controlled in terms of distribution and spatially show slightly higher values toward the edge of the wafer. This data is reinforced with maximum source drain currents shown in Figure 9. Maximum values are again clustered towards the edge of the wafer and 90% yields for both of these values show the potential for high yields over large areas. Compared to equivalent devices built on GaN on silicon wafers the values are slightly low which may be due to differences in composition of the channel layer or stress in the films. This issue remains to be investigated in detail.

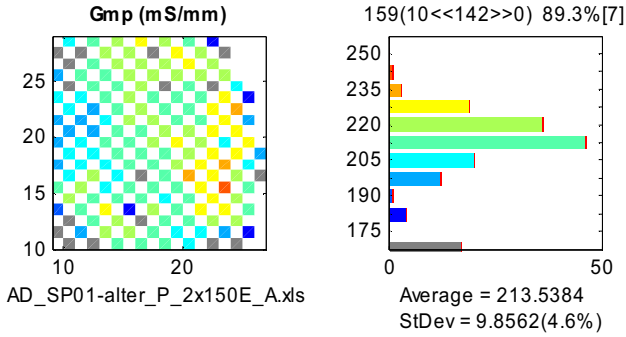

Figure 8
Gain (Gm) – wafer 1

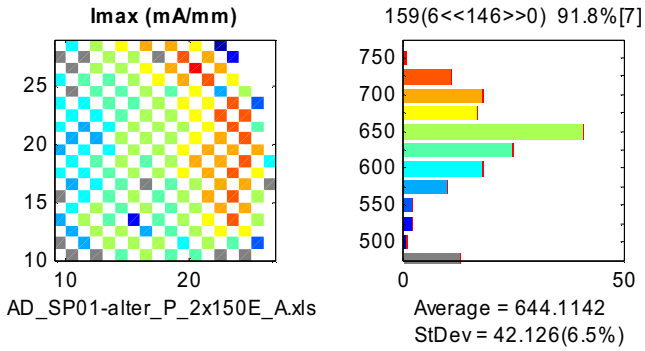

Figure 9
S/D Imax – ma/mm – wafer 1

Finally, if the frequency response of the devices is measured, we find that the values are consistent with the measured device geometry. Figures 10 and 11 show values and distributions for f_{max} and f_t. Again, defective die are randomly distributed and lower values are clustered toward the edge of the wafer where gate lengths were slightly longer.

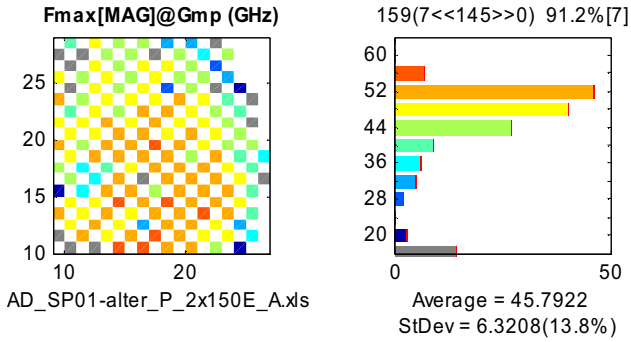

Figure 10
Fmax – wafer 1

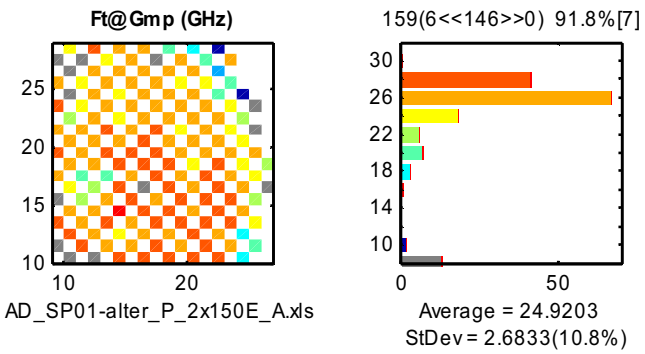

Figure 11
Ft – wafer 1

Values and distributions of these parameters for wafer 2 were similar although slightly lower but still demonstrated that reasonable yields of functional devices could be achieved.

Significant work remains however. Figure 12 shows the pulsed IV characteristics of a device where significant thermal droop is evident. This measurement was done on a full wafer which had not yet had the silicon handle wafer removed but it clearly shows the necessity of performing this step so that the diamond layer is in direct contact with a cooled surface.

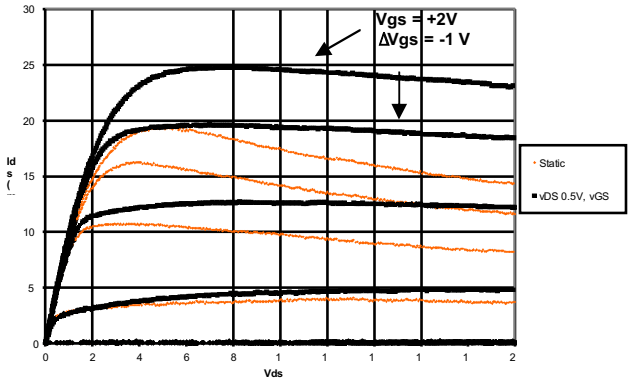

Figure 12
DC and pulsed IV plot showing thermal droop

The high Young's modulus of diamond allows the complete removal of the silicon handle wafer which was used for processing the wafer and this leaves only three layers between the device junction and the package. Figure 13 shows a cross section of this structure where the stack consists of the GaN epi layer, the silicon buffer layer used for the GaN growth, and the diamond substrate.

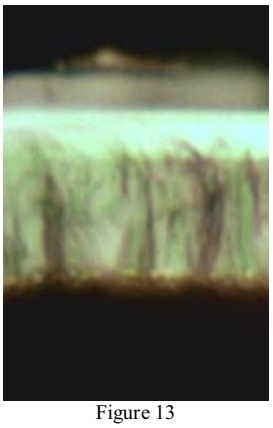

Figure 13
Cross section of die after handle removal showing GaN, silicon and diamond layers

CONCLUSIONS

GaN HEMT devices on thermally conductive diamond substrates provide a path for increasing both power dissipation and reliability. They must be fabricated at high yield on large diameter wafers to meet manufacturing economic goals however. This work has now demonstrated that these devices can be fabricated on 100 mm wafers with yields sufficient to meet manufacturing goals. Both spatial consistency and acceptable variation in parametric values was achieved on more than one wafer. Much remains to be done to reach full manufacturing readiness but there do not appear to be any blocking issues in implementing this technology on a variety of compound semiconductor devices including power RF, power switching, high luminance LED's and VCSEL laser diodes..

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ACRONYMS

SOD: Silicon on Diamond
HEMT: High Electron Mobility Transistor
GaN: Gallium Nitride