

# HBT Epitaxial Material Matching and Qualification for High Volume Production

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## Abstract

**Reliable and reproducible epitaxy (epi) materials are critical to the success of a high volume compound semiconductor fabrication line. An efficient epi matching and qualification procedure among different epi reactors and suppliers is paramount to supporting rapid fab capacity ramp to keep pace with market demands. Traditional methods of individual layer thickness and doping matching, such as Secondary Ion Mass Spectroscopy (SIMS), have limitations when applied to heterojunctions and subtle interface matching. Sometimes a subtle epi interface mismatch can create significant discrepancies in transistor characteristics and RF module performance. Multiple iterations of lengthy epi matching as well as RF module level characterization may be required to resolve the differences. To overcome these limitations, we developed an epi matching procedure which greatly shortened the cycle time for epi qualification. After an initial “quick-lot” matching is performed by our suppliers, extensive transistor level electrical data is collected and compared to the historical production distribution. The measured data of these qualification samples must be within 2.5 sigma of the historical distribution with the same mean. The in-line DC PCM parameters, for the technology generation, are a subset collected data. In addition, an extended set of DC and RF parameters is also matched within the same stringent criteria. After the transistor level electrical data fully matches the historical distribution of our database, the qualification samples then go through transistor level reliability and module level evaluations. Adequate transistor level reliability and comparable module level performance are required for a full production release of a new epi reactor.**

## INTRODUCTION

Over the past decade, GaAs-based Heterojunction Bipolar Transistors (HBTs) have solidified their position as the technology of choice for fabricating wireless handset power amplifiers (PAs). A number of cost/performance factors have enabled compound semiconductor devices to outperform silicon, and other competing technologies for wireless PA applications. In particular, on-going

improvements in yield, fabrication cycle time, and cost have kept GaAs technologies at the leading edge by delivering cost and performance improvements for PA modules (PAM) and front end modules (FEM). Skyworks is well positioned to develop and rapidly introduce novel high performance and cost competitive PAMs and FEMs to the market based on the strength of our internal compound semiconductor fabs. A critical factor to the success of a high volume GaAs fabrication line is the quality and consistency of the starting epitaxial materials. This is especially important when running a GaAs production line at maximum capacity. Under these circumstances, there is neither time nor fab capacity to recover from any yield incidents related to starting epi. A single batch of non-conforming starting epi could have irrecoverable impact on quarterly revenue targets.

Previous methods made qualification of new reactors and/or epi-suppliers a lengthy process with low success. These old procedures relied heavily on SIMS characterization, minimal in-line process control monitor (PCM) data, and module level characterization. They also relied on comparison to controls rather than to a historical distribution. As a result, material vendors typically faced formidable barriers that hindered the adoption of their materials in high volume products. This approach had the disadvantages of making the feedback time very long and often ambiguous since the PCM data was not suitable to identify subtle differences in materials – even from the same vendor. That approach ultimately leads to higher cost epi (due to availability) and made it virtually impossible to rapidly ramp capacity to meet market demand. To improve the success rate and speed of new reactor and vendor qualifications, we developed a novel and highly efficient epi qualification procedure at the Skyworks Newbury Park fab.

A key principle for this work was to MATCH the currently released materials, not “improve” them. In effect, different=bad. A second important principle was that we needed to go through this process of device and circuit level matching without requiring any design resources to re-tune parts. For our designers and product engineers, the materials need to be matched closely enough that they don’t require different electrical specs, models, or binning (pairing of material and product). This saves a lot of “non-value added”

logistic work and reduces chances of error. From our customer's standpoint, the accurate matching of materials results in predictable, consistent material supply and products with less variation. This means that we are really delivering the same product (in terms of performance), independent of the reactor or material source. Feedback we have received from our customers indicates our parts are, in fact, more consistent than our competitors.

The main steps in the matching procedure are (1) communicate "quick-lot" (QL) expectations, including characterization algorithms, with the material suppliers to ensure that they match the historical QL data before we run any material in our fab, (2) perform detailed device characterization and provide timely feedback on matching, (3) only after the materials are matched does module level characterization proceed.

Using this improved epi qualification process, the average time required to qualify a new epi reactor was shortened from 12 months to 3-6 months and new epi supplier qualification from 2 ~3 years to 6 ~ 9 months. This same philosophy used in material matching can, in principle, be applied to component and laminate qualification.

#### CONVENTIONAL APPROACH FOR EPI MATCHING

##### A. Limitations to SIMS matching

In the compound semiconductor material growth industry, epi suppliers rely on characterization techniques such as, Double Crystal X-Ray Diffraction (DCXRD), Hall measurements, and Photoluminescence (PL) to determine epitaxial layer quality, growth rate, alloy compositions and doping, whereas manufacturers are interested in the resulting electrical characteristics - which can only be obtained by processing small area devices. Since various epi suppliers have different calibration standards, Secondary Ion Mass Spectroscopy (SIMS) matching was previously used as the primary technique for epi material matching. This allowed individual epi layer thicknesses, doping and alloy

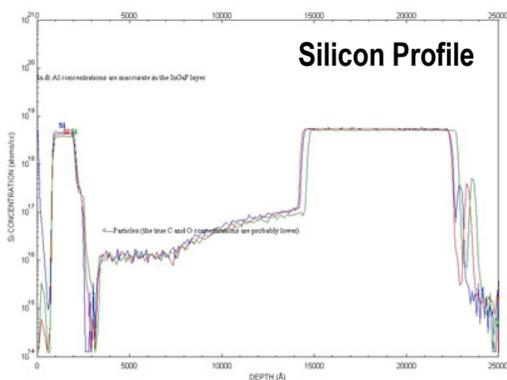


Fig. 1. SIMS matched silicon doping profiles within an InGaP HBT structure from two different epi suppliers and three different MOCVD reactors

compositions among different suppliers to be compared. As shown in Fig. 1. SIMS data may provide adequate information to match individual layer thickness and doping; however, SIMS provides limited information on critical, and often subtle, interface transitions and heterojunction properties.

Fig. 2 shows an example of mismatched transistor characteristics of "SIMS matched" samples from 5 different epi suppliers. In addition to these limitations, SIMS measurements are a long lead time service normally reserved for trouble shooting the epitaxial growth rather than serving as a calibration tool. Because of these drawbacks, we found a perfect SIMS match would not guarantee a transistor level electrical performance match.

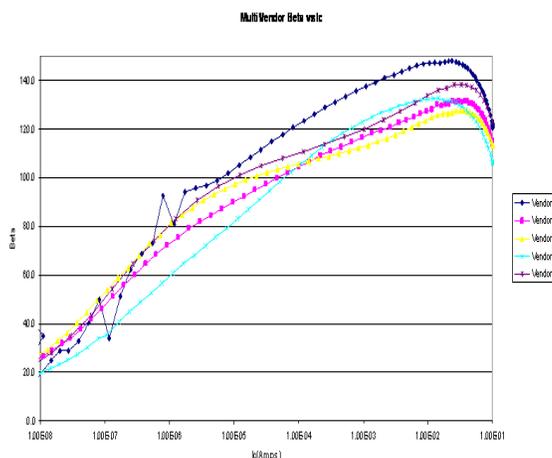


Fig.2. Beta vs. Ic curves of "SIMS matched" samples from five different epi suppliers

##### B. Limitations to Quick Lot (QL) measurements

A "quick-lot" QL process [1] is often used by HBT epi suppliers to ensure that the wafers they ship to the customer meet desired specifications. From these crude, large area devices, a few HBT electrical parameters such as beta, turn-on, and sheet resistances can be monitored and reviewed before circuit fabrication. Failure to implement this sort of QL strategy can result in costly yield issues since data will not be available until after all of the cost and effort of fully processing the wafer. For a qualified epi supplier, QL measurements can provide valuable electrical information and show excellent correlation with much of our final PCM data. However, QL data alone is inadequate for epi matching since the large area devices cannot be driven to high current densities. Many critical device parameters including emitter resistance, transit time, ft and fmax, and small area capacitances cannot be measured from a simple QL device. Therefore, unfortunately, QL data meeting all the required specifications is necessary but not sufficient to guarantee a good epi match.

### C. A lengthy cycle for data feedback

Another serious problem associated with this traditional epi matching approach is a very lengthy cycle time for data collection and feedback. Fig. 3 shows the flow chart of a previous epi qualification procedure. Based on the old qualification procedure, the time required for a set of qualification samples from an epi supplier was typically 4-6 weeks due to the requirements of SIMS matching. Fab processing, PCM measurements and transistor level reliability evaluation would take another 6-8 weeks. In general, the data collected at this point would not show any signs of trouble. The wafers were then sent to assembly for module build and functional test. Occasionally functional test would exhibit yield differences between the control sample and the qualification samples. At that point, epi suppliers would be asked to re-submit samples to go through this process again after 4 months of waiting! More frequently, the worst case situation would be a mismatch found in module level characterization data. As we know, module level characterization is very resource limited and typically has long lead time (> 1 month). Detecting any epi related performance differences at this step, means 5-6 months of effort and resources would have been wasted. Worse, the entire process has to be repeated until it works. Such a long data feedback cycle time coupled with the uncertainty of SIMS matching and QL data matching made the old epi qualification an inefficient and cumbersome process. Since more than two iterations were usually required for each qualification, an average epi qualification cycle time could easily take more than 12 month, which was indeed the case.

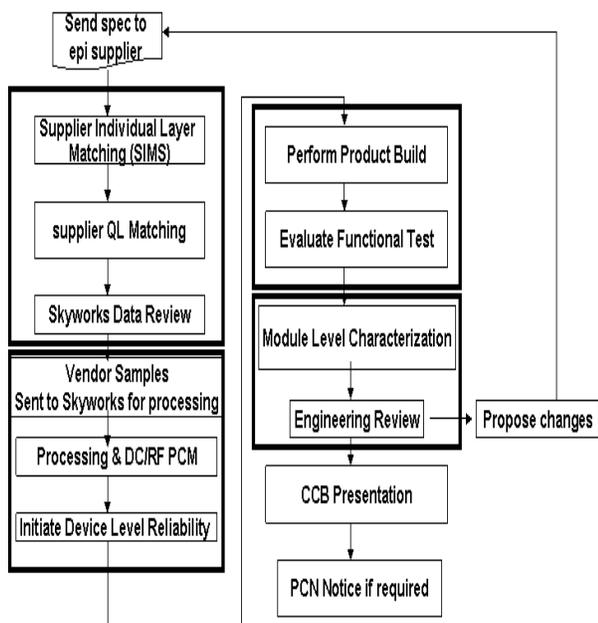


Fig.3. An old epi qualification process flow chart

### NEW EPI QUALIFICATION PROCEDURE

An epi technical team was formed and tasked with improving the epi qualification process and reducing qualification cycle time. This team reviewed the existing process and proposed modifications to the data review and feedback procedure. Fig. 4 shows the flow chart of an improved epi matching procedure that was proposed and later adopted. To detect any epi discrepancies at an earlier stage, instead of relying on module level characterization, transistor level electrical data of samples to be qualified is collected and compared to the historical production distribution. The measured data of the qualification samples must be within 2.5 sigma of the historical distribution with the same mean. Viewing this data on a probability plot gives a visual indication of whether or not given parameters are getting closer to matching or not. The DC PCM parameters for the technology generation which the material to be used are a minimum set of parameters.

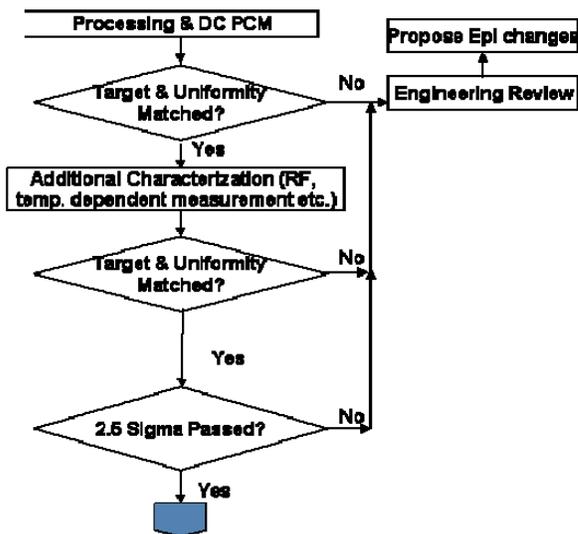


Fig.4. A simplified epi matching process flow chart

In addition, an extended set of electrical parameters as shown in Table I, must be matched within the same stringent criteria. This extra level of measurements was used to monitor parameters which could affect circuit performance as well as HBT transistor model parameters (in addition, full IV curves were also reviewed). If any of these critical parameters fail to meet the 2.5 sigma criteria, we feedback the data and the failed parameters back to the epi suppliers. After the transistor level electrical data of the qualification samples fully matches the historical distribution of our database, the qualification wafers undergo transistor level reliability evaluation and need to pass the reliability requirements. This step is not performed in parallel to

device testing since there are a limited number of fixtures for device level reliability. However, wafers are sent, in parallel, to reliability testing and to assembly for PAM builds. Initially module characterization comparisons are still required. After 100% success rate of the new 2.5 sigma approach, the product engineering team agreed to remove the requirement of full module characterization. Final PAM product yield now serves as the final gate for a new epi reactor qualification. A comparable final product yield with similar module performance is the new criteria to pass the new epi reactor qualification.

TABLE I

| Electrical Parameters                    |                                  |
|--|----------------------------------|
| Vce_sat(V)                               | Iscl                             |
| Beta @ 0.01 mA/um <sup>2</sup>           | BEIk (A)                         |
| Beta @ 0.1 mA/um <sup>2</sup>            | BCIk (A)                         |
| Beta_max                                 | Vbc3 (V)                         |
| Jc @ Beta_max (mA/um <sup>2</sup> )      | Vbe @0.01 mA/um <sup>2</sup> (V) |
| Beta drift @0.01 mA/um <sup>2</sup>      | Vbe @0.1 mA/um <sup>2</sup> (V)  |
| Beta drift @0.1 mA/um <sup>2</sup>       | Re_flyback (Ohms)                |
| Nfb                                      | Ref (Ohms)                       |
| Nfc                                      | Phi*Rth (A-1)                    |
| Nfbl                                     | Rc_flyback (Ohms)                |
| Nfcl                                     | Cjc (fF) @0V                     |
| Isbl                                     | Cje (fF) @0V                     |
| ft (GHz) @0.01 mA/um <sup>2</sup> & 1.5V | K @ 1.9GHz                       |
| ft (GHz) @0.1 mA/um <sup>2</sup> & 1.5V  | H21  (dB) @ 2.4GHz               |
| ft (GHz) @0.25 mA/um <sup>2</sup> & 1.5V | MSG/MAG (dB) @ 2.4GHz            |
| hFE @0.1 mA/um <sup>2</sup> & 3.5V       | U (dB) @ 2.4GHz                  |
| Tau @ 1.5V                               | K @ 2.4GHz                       |
| H21  (dB) @ 900 MHz                      | H21  (dB) @ 5.8GHz               |
| MSG/MAG (dB) @ 900 MHz                   | MSG/MAG (dB) @ 5.8GHz            |
| U (dB) @ 900 MHz                         | U (dB) @ 5.8GHz                  |
| K @ 900 MHz                              | K @ 5.8GHz                       |
| H21  (dB) @ 1.9GHz                       | U (dB) @ 1.9GHz                  |
| MSG/MAG (dB) @ 1.9GHz                    |                                  |

A special set of electrical parameters related to circuit performance and HBT transistor modeling parameters

## RESULTS AND DISCUSSIONS

The cycle time for data analysis and feedback to epi suppliers was greatly reduced from over 5 months to approximately 4 weeks in this new epi qualification procedure. We also removed the requirements of SIMS matching after discussions with several epi suppliers and experts in the fields. Eliminating the SIMS matching requirement allows epi suppliers to reduce the time required for qualification samples preparation to 2-3 weeks. With a greatly shortened data feedback time and a reduced qualification sample preparation time, a typical epi reactor

qualification can be achieved within three to four months.

In the past two years, by using this improved epi qual process, we have greatly increased the InGaP epi capacity from below 1500 wafers per week to over 3500 wafers per week by qualifying multiple MOCVD reactors at our 4" epi supplier. Also taking advantage of the recent Skyworks 6" conversion in Newbury Park and the availability of an efficient epi qualification procedure, we are adding an additional epi supplier for our 6" HBT wafers. Qualifying an additional epi supplier not only provides more flexibility in capacity planning but potentially achieves a better balance between incoming epi quality and pricing. 6" HBT samples from one of the epi suppliers were fully matched to our historical distribution in two iterations.

## CONCLUSIONS

We have developed a highly efficient epi qualification process by linking epi qualification to transistor level electrical parameters instead of layer by layer matching. This approach has greatly shortened the epi qualification cycle time. Over 2000 wafers per week new capacity has been added by this process in the past two years. Also we qualified two 6" epi suppliers in a record short time. A similar philosophy should be possible with other externally purchased materials such as components and laminates.

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## ACRONYMS

- HBT: Heterojunction Bipolar Transistor  
SIMS: Secondary Ion Mass Spectroscopy  
PAM: Power Amplifier Module  
FEM: Front End Module