

Dramatic Reduction of Surface Defects and Particles on pHEMT epi-wafers grown by MOVPE for higher yield of Transistors

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Keywords: GaAs, pHEMTs, epi-wafers, MOVPE, surface defects,

Abstract

A dramatic reduction in the defect density has been achieved on 6" diameter pHEMT epi-wafers by using face down type MOVPE reactors. The defects were analyzed and found to come from deposition in the reactor. The deposition temperature was varied the experiment and found it was occurred in lower temperature than we thought, under 250C incase we used TEG. Based on these results, the temperature distribution of the reactor was redesigned. As a result, defect density was reduced to the extremely low value of 0.2/ cm².

INTRODUCTION

The GaAs-pHEMT is widely used for high frequency switching devices in wireless systems like cellular phones, W-LANs, GPS, etc. The new generations of cell phone of 3G, 3.5G contain multiple transceivers with different modulation formats, so the pHEMT switch ICs in the RF path must connect to a large number of nodes (e.g., SP9T or more). This trend drives an increasing complexity of the pHEMT switch ICs in these phones, and requires improvements in surface cleanliness and defect reduction in the pHEMT epi wafers in order to maintain high IC yields.

The pHEMT epi-wafers are generally grown by either MBE or MOVPE. Wafers grown by MBE have "oval defects"^{[1][2]} with a density of 50 to 100/cm² if we count the defects over 0.5 μm size. Oval defects can form because of incomplete desorption of surface oxides from substrates which locally interfere with epi growth, and also from spitting of defects by the Ga cell. Fortunately, MOVPE has no such epi growth related defects when clean substrates are used. The defect density for MOVPE wafers is usually less than 20/cm², and that mainly comes from particles. In this work, we focused on reduction of particles to achieve further reduction in defect density of our MOVPE pHEMPT epi wafers.

REACTOR DESIGN AND DEFECT DENSITY BEFORE IMPROVEMENT

There are many kinds of MOVPE design, as shown in Fig.1. Most MOVPE reactors on the market are the "face up" type (see Fig. 1). In this work, we used the "face down" type of reactor, where the epi surface is facing downward^[3]^[4] to prevent particles from falling onto the wafer surface. In this paper, we used a "face down" planetary reactor, which can grow six 6inch wafers at a time, providing the high throughput needed for production.

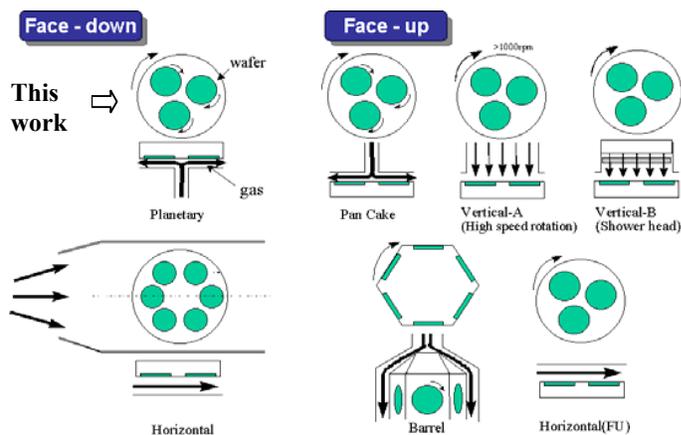


Fig.1 MOVPE systems

The 6" dia pHEMT epi-wafers were grown using our "face down" planetary reactor, and using TMG, TEG, TMI, TMA, arsine and Phosphine as the precursors. The defect densities, as measured by a Surfscan particle counter, were typically less than 5/cm², but the occasionally increased to 20 cm², as shown in Fig 2. Some part has high density defects.

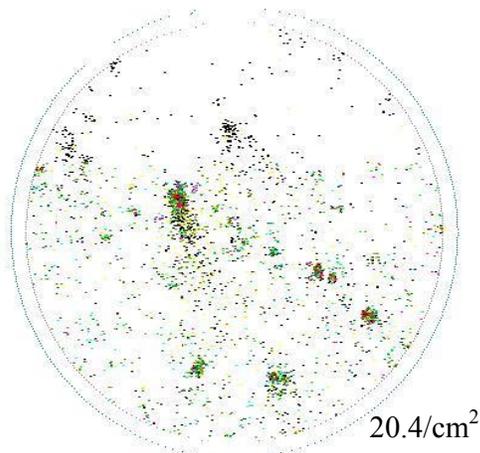


Fig.2 Defect map over 0.5um diameter of 6" pHEMT "bad" wafer. Density of defects is 20.4/cm²

ANALYSIS OF THE PARTICLES

The particles on the wafers were analyzed by SEM-EDX to determine what atomic species were present, and to find out possible origins for the particles. A total of 10 particles from different wafers with different growth runs were analyzed by SEM-EDX, and Fig. 3 shows typical EDX spectrum of a particle.

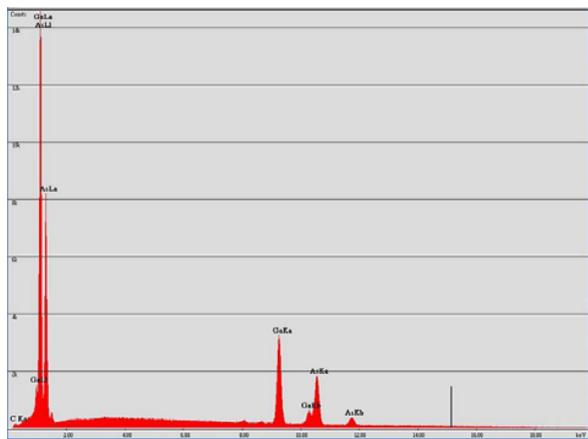


Fig.3 EDX signal from the particle

Only Ga and As were detected from the EDX spectra of most particles (see Fig.3). A small In peak was seen in the EDX spectra of some particles. From this data we conclude that all the particles were composed of semiconductor material, and they did not come from external contaminants or particles from parts of the reactor itself. We propose that this semiconductor material had originally been deposited on the reactor wall, and it then detached and was transported to the epi wafer surface. (Most such particles would presumably fall downward away from the wafer, but a few

apparently are still transported to the "face down" epi surface. We must study the specifics of the deposition to understand how to reduce these particles.

The characteristics of the semiconductor wall deposits in the reactors was carefully observed in everywhere in the reactor after long-run growth (around one month). Most of the semiconductor wall deposits were firmly attached, like a good coating, seemed unlikely to detach and cause particles on the wafers. However, we also found semiconductor wall deposits which appeared less firmly attached in cooler regions of the reactor. These regions operate at temperatures less than 350C, so it was somewhat surprising to find any semiconductor deposition there at all. However, the morphology of these deposits and the low temperature of the deposition zone, suggested that depositions in these cool regions might be the origin of the particles.

EXPERIMENT OF DEPOSITION

To further understand the influence of temperature on the characteristics of semiconductor wall deposits in an MOVPE reactor, several experimental depositions were done at various temperatures in a small experimental MOVPE reactor. Films of GaAs, InAs and InGaAs were grown on GaAs substrates, as well as on graphite, and on quartz substrates, over a wide temperature range from 150C to 630C. The usual precursors for these materials were used, namely TMG and TEG for Ga, TMI for Indium and Arsine for As. The deposition rate was measured on all the samples.

Deposition occurred on the GaAs substrate, the graphite, and the quartz with almost same growth rates. The temperature dependence of growth rate for each type of deposited semiconductor is shown in Fig.4.

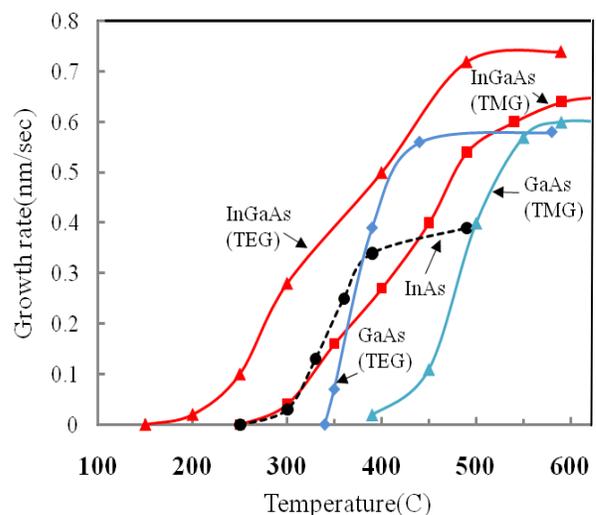


Fig.4 Growth rate of each materials on quartz plate.

It was found that depositions of the semiconductors containing Indium occurred at surprisingly low temperatures (i.e., less than 330 C). The deposition of InGaAs using TEG as the Ga precursor showed the lowest deposition temperature of 250C. This is a much lower temperature than we expected for the threshold temperature for the onset of deposition.

We also checked the stability of deposited film, by testing how easily it would detach from the substrate when touched. Phosphine was also added in this investigation as P source. The depositions that contained either In and/or P were qualitatively less stable at low temperature growth than those without In or P.

IMPROVEMENT AND RESULTS

The knowledge that semiconductor wall deposits of the epi materials of interest could form at much lower temperatures than previously expected was used to improve the MOVPE thermal design. This knowledge was used to modify and optimize the detailed temperature profile in the MOVPE reactor to minimize wall deposits. In some parts of the reactor, the temperature was reduced to prevent deposition, and in other parts of the reactor, the temperature was increased to make the wall deposits more stable.

This improved MOVPE reactor has now been used in the mass production of 6" pHEMT wafers. Fig.5 shows the defect map of one of the epi-wafers. The density was very low of 0.06/cm² and the localized high density part could not be seen at all.

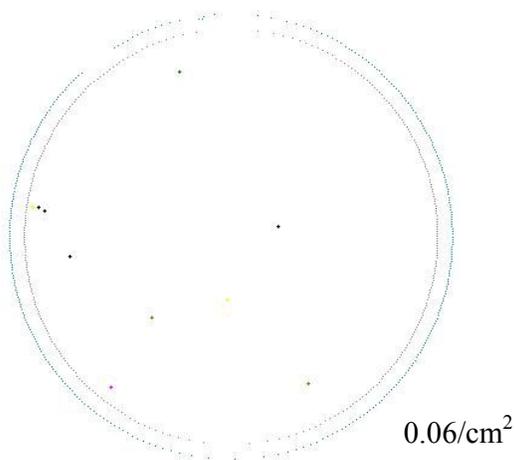


Fig.5 Defect map over 0.5um diameter of 6" pHEMT improved wafer. Density of defects is 0.06/cm²

A histogram of the defect density of about 3000 wafers is shown in Fig.6. The average density is 0.2/cm² and most of the wafers have lower than 1/cm². The improvement of

the reactor gave us the dramatic decrease of the defect density. This large reduction in defect density is expected to provide a correspondingly higher yield for pHEMT switch ICs.

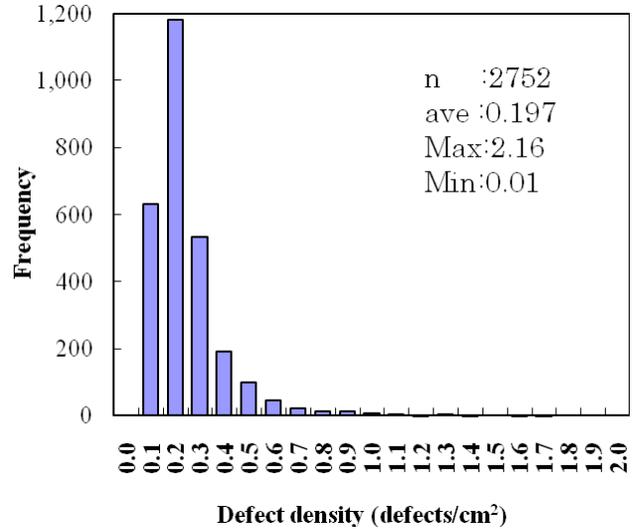


Fig.6 Histogram of surface density on the 6" pHEMT epi wafers grown by the improvement reactor

ESTIMATION OF DEFECT REDUCTION EFFECT

The effect of the defect density reduction was calculated. When defects scattered in a wafer as Poisson distribution, the probability P of no particles fallen within the IC's "defect sensitive area", where defects cause fatal damage, like FETs and capacitors is calculated in equation (1);

$$P = \exp(-D.A.S) \dots (1)$$

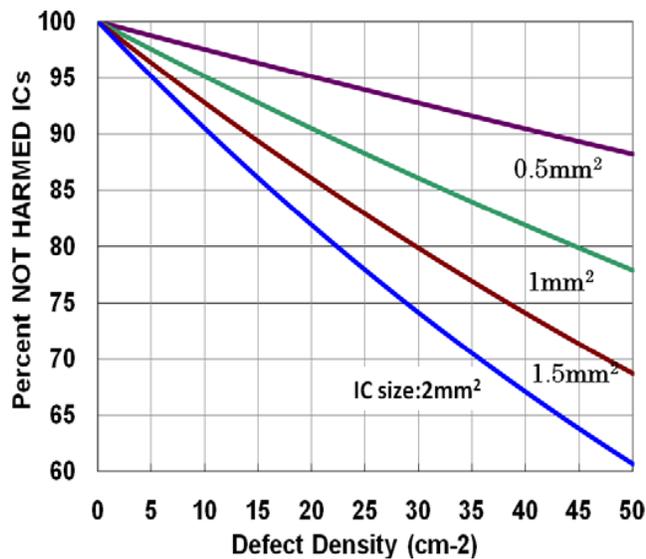
Where

D: defect density

A: IC size

S: Ratio of defect sensitive area in the IC area A.

The calculation result is shown in Fig. 7 in case the ratio S is 50% and device size A is from 0.5 mm² to 2mm². Ration of not harmed IC, which must has strong relation with IC yield, is influenced a lot by the defect density especially in a large device size like 2mm² (SP9T is this range generally). The device yield is determined by many parameters, not so simple, but it's clear the surface defects density has big impact on the yield especially for the large device.



GPS : Global Positioning System
 TMG: Trimethyl Gallium ((CH₃)₃Ga)
 TEG : Triethyl Gallium (C₂H₅)₃Ga)
 TMI : Trimethyl Indium(CH₃)₃In)
 TMA : Trimethyl Aluminum (CH₃)₃Al)
 SEM: Scanning Electron Microscope
 EDX: Energy Dispersive X-Ray

Fig.7 Calculation result of defect density influence on ICs
 Where ratio of “defect sensitive are in IC is 50%.

CONCLUSION

The surface defects on epi-wafers grown by “face down” MOVPE was determined to originate mainly from semiconductor particles coming from unstable wall deposits inside the reactor. This wall deposition was found to occur at the surprisingly low temperature of 250C in the case TEG was used as a Ga source, and as low as 300C for TMG grown InGaAs. Based on the results, the temperature distribution for the reactor was optimized, and the modified reactor has produced a very low defect density of 0.2/ cm² average in the mass production of 6” pHEMTs. This large reduction in defect density can be expected to provide a corresponding improvement in yield for pHEMT switch ICs.

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ACKNOWLEDGEMENT

Authors appreciate Tom Low of Agilent for very useful discussion for whole area of this paper.

ACRONYMS

GaAs: Gallium Arsenide
 pHEMT: pseudomorphic High Electron Mobility Transistor
 MOVPE : Metal Organic Vapor Phase Epitaxy
 MBE : Molecular Beam Epitaxy
 W-LAN : Wireless Local Area Network