pHEMT Switch Yield Improvement Through Feedback From 100% Die Test

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Abstract

Yield improvement is an ongoing process in the MMIC production line. The gate lithography process will determine the major part of pHEMT wafer yield. This paper investigates yield improvement through feedback from automatic 100% DC and switching time on wafer testing. The breakdown and time domain test provides a reticle-dependent distribution pattern. This is photolithography process dependent and has been attributed to defocus during stepper exposure at gate level. Feeding this information back to the process engineers enables them to pinpoint the specific process step and improve the process yield.

INTRODUCTION

100% automatic visual inspection (AVI) [1] is a useful tool to screen out defective dies due to processing issues, including metal scratches, metal peeling, deformed gates and broken gates. The majority of the yield loss (around 80%) can be detected by AVI and attributed to gate voids and broken gates. However, certain types of gate defects caused by minor defocus during gate lithography result in gate distortion and gate lag that cannot be screened out by physical AVI. In the worst scenario, these types of defects could cause 15% of die yield loss. In this paper, we develop a DC and time domain test system to screen out dies with gate distortion and gate lag [2-5]. The system provides yield bin map, mean and standard deviation variances of key parameters from the 100% wafer level die sort test.

Thus, process engineers are able to determine which specific process step has gone wrong in the highly complicated pHEMT switch fabrication flow which will result in reduction of yield excursion and increased yields.

EXPERIMENTAL

AVI can screen out defective dies due to processing issues such as defective gates (Figure 1a) or broken gate fingers (Figure 1b) that would cause poor or failed pHEMT switch performance. In order to be able to sensibly compare AVI and IDSS maps, we ran tests to determine both the appropriate magnification for AVI as well as proper IDSS thresholds dependent on the specific gate array area. Some critical areas defined for AVI are: (i) Gate Channel: The area between drain and source of the transistor; (ii) Gate Finger: The area of the transistor that consists of multiple gate stripes.

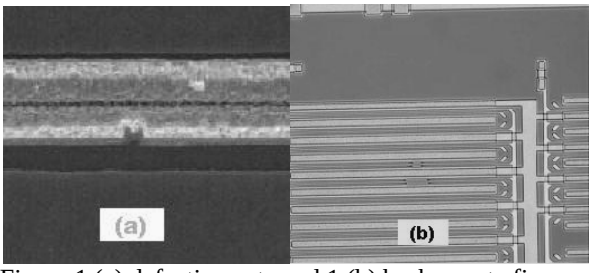

Figure 1 (a) defective gate and 1 (b) broken gate fingers.

An experiment was designed to explore the relation between AVI and the developed DC screen test. AVI will screen the whole six-inch wafer after gate metal formation. The DC test will screen for electrical failures (parameter out of specification limits) after the complete process is finished.

The experimental steps included: (A) add AVI monitor stage after gate metal formation and three chip probing (CP) test stages: (B) IDSS test, (C) breakdown test and (D) time domain test as shown in Table 1:

Table 1: Experiment stages and description.

Check point	Description	Tool
A	After Gate metal formation	AVI
B	CP test_IDSS	DC source
C	CP test_IDSS_breakDown	DC source
D	CP test_IDSS_Time Domain	DC source and Signal Generator

TEST SYSTEM SETUP

There are four blocks in the test system as shown in Figure 2: The DUT is placed on EG 4090u prober. The Signal Generator block includes Time Measurement

Counter (TMU) and Arbitrary Waveform Generator (AWG). The DC Source block will supply four Precision Measurement Unit (PMU) channels. The Oscilloscope monitors switch time and voltage of a signal pulse in the DUT.

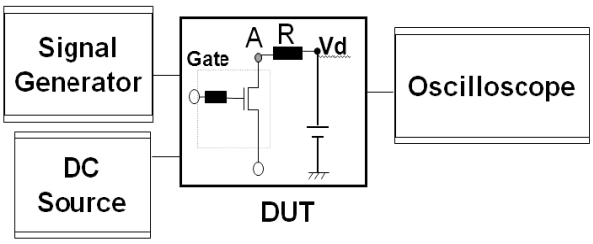

Figure 2: Test system setup.

The DC source delivers the measurement accuracy for low-current IDSS test and capability required for high breakdown voltage test. The time domain measurement is made by triggering the device with the AWG and using the TMU to measure the switching time. The resistor R is set from 50ohm to 250ohm for current limiting and is chosen according to circuit design.

RESULTS AND DISCUSSIONS

Figure 3 shows the AVI wafer map generated at check point A. Figure 4 shows the map at check point B after the DC sorting IDSS test. Comparing of AVI map and DC IDSS test wafer map revealed identical pattern clearly demonstrating that gate voids and broken gates can be screened by both methods. It also shows the suitability of the specified magnification range for AVI and test limits for IDSS test.

However, check points C (Figure 5) and D (Figure 6) show reticle-like patterns that are not observed from check points A or B. It means that some of the process defect phenomena such as gate distortion and gate lag caused by a slight gate lithograph defocus cannot be screened by 100% automatic visual inspection. Fortunately, these two unfavorable process problems can be sorted by wafer level die test.

Chips with gate distortion can be sorted by forcing a reverse bias current through the gate and measuring breakdown voltage of chips. Figure 5 shows the reticle-dependent wafer map of the measured breakdown voltage distribution across a six-inch wafer. Within a reticle the breakdown value gradual increases from right bottom to left top corner.

The time domain test method is implemented to sort the chips by gate lagging time that directly influences the switching time of the antenna switch. The test plan is performed in the following sequence. Firstly, we set a reference voltage (Vref) at point A on the DUT. Then a pulsed signal at the gate changes the transistor from off state to on state. We calculate the drain transient time during the drain voltage drop from high voltage to Vref voltage. Figure 7 shows the drain transient time test result from the oscilloscope. It is well known that the drain transient time is related to the gate's surface states and depletion region. The slow response of surface states to the signal is the major source of the gate lag. Developing a stable and consistent gate process to suppress gate lag is one of the most critical parts in pHEMT switch process development. Figure 6 shows the reticle-dependent wafer map of the measured drain transient time distribution across a six-inch wafer. Within a reticle the drain transient time value shows a gradual decrease from right bottom to left top corner.

Both breakdown and transient time test distribution are clearly photolithography process dependent and have been attributed to defocus during stepper exposure at gate level.

It is sometimes a difficult task for a process engineer to determine which specific process step in the highly complicated pHEMT switch fabrication flow causes the poor switching time. By analyzing the wafer map generated from the die testing methodology described above, the process engineers are able to quickly pinpoint the specific process step that causes switching time drift in unfavorable direction. Figures 8 and 9 are wafer maps for breakdown voltage and drain transient time after the gate process parameters have been re-optimized according to the feedback from the die test wafer map. The absolute value of the switching time is improved by a factor of 4.5 and across-wafer standard deviation for switching time is also improved by a factor of 5. No reticle dependent wafer map was observed anymore.

CONCLUSIONS

In this paper, we have demonstrated an DC and time domain test system related to gate distortion and gate lag that cannot be screened out by physical AVI. The process engineer then optimized the process for normal distribution in high breakdown and low gate lag test results according to the test feedback. No reticle dependent wafer map was observed anymore and the overall die yield is improved by 15%.

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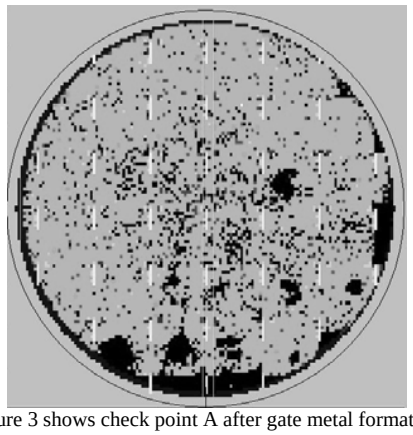

Figure 3 shows check point A after gate metal formation.

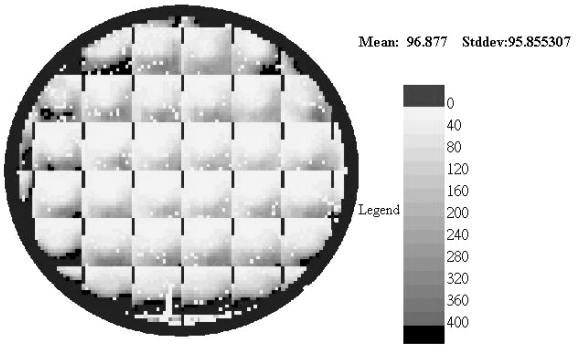

Figure 6 shows the reticle-dependent wafer map of the measured drain transient time distribution across a six-inch wafer.

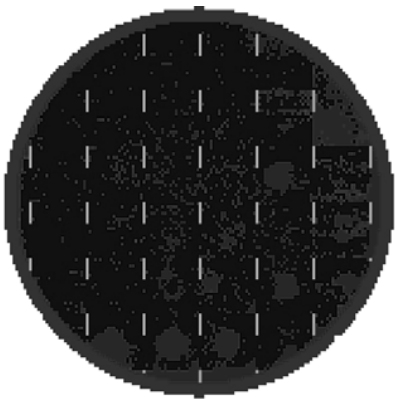

Figure 4 shows check point B after the DC sorting IDSS test.

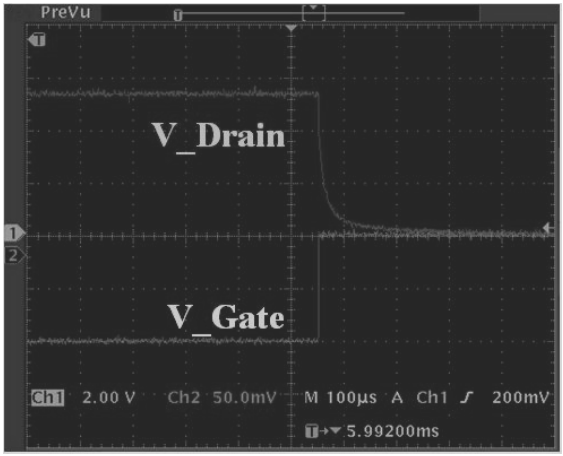

Figure 7 shows the drain transient time test result from the oscilloscope.

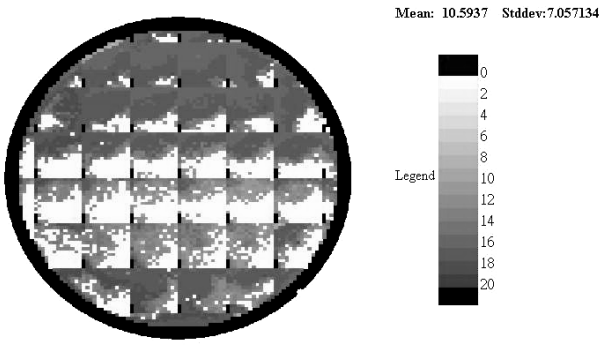

Figure 5 shows the reticle-dependent wafer map of the measured breakdown voltage distribution across a six-inch wafer.

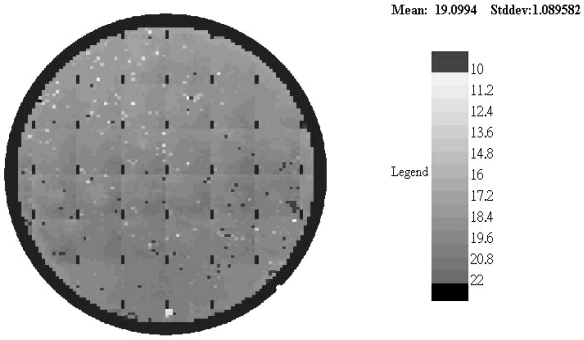

Figure 8 shows the wafer map for breakdown voltage after the gate process parameters were re-optimized.

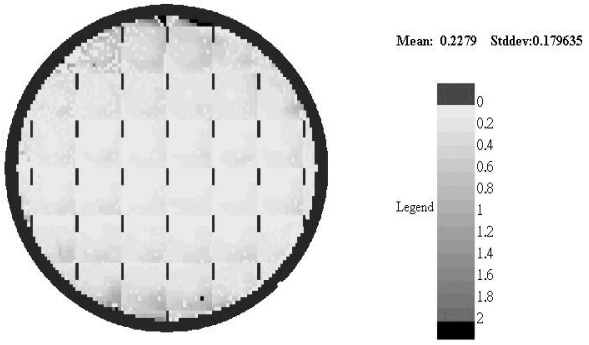

Figure 9 shows the wafer map for drain transient time after the gate process parameters were re-optimized.

REFERENCES

[1] Y.Z. Wang, R.S. Persaud, R.C. Salvador, D. J. Troy, Statistical Quality Control of Wafer Level DC Die Sort Test 2006 GaAs MANTECH Technical Digest,pp. 79-82, Apr 2006.

[2] Y. Mitani, D. Kasai, K. Horio, Analysis of surface-state and impact ionization effects on breakdown characteristics and gate-lag phenomena in narrowly recessed gate GaAs FETs, *IEEE Trans. on Electron Devices*, 50, pp. 285–291, 2003.

[3] E. Tediosi, M. Borgarino, G. Verzellesei, G. Sozzi, R. Menozzi, Surface effects on turn-off characterisitcs of AlGaAs/GaAs HFETs, *ElectronicLetters*, 37, pp. 719–720, 2001.

[4] S. H. Lo, C. P. Lee, Analysis of surface state effect on gate lag phenomena in GaAs Mesfet's, *IEEE Trans. on Electron Devices*, 41, pp. 1504–1512,1994.

[5] K. Horio, T. Yamada, Two-dimensional analysis of surface-state effects on turn-on characteristics in GaAs MESFETs, *IEEE Trans. ElectronDevices*, 46, pp. 648-655, 1999.

ACRONYMS

pHEMT: pseudomorphic High Electron Mobility Transistor
MMIC: Microwave Monolithic Integrated Circuit
AVI: Automatic Visual Inspection
TMU: Time Interval Counter
AWG: Arbitrary Waveform Generator
PMU: Precision Measurement Unit