Monolithically Integrated III-V and Si CMOS Devices on Silicon on Lattice Engineered Substrates (SOLES)

J.R. LaRoche, W.E. Hoke, and T.E. Kazior
Raytheon Integrated Defense Systems, Andover, Massachusetts, USA

D. Lubyshev, J. M. Fastenau, and W. K. Liu
IQE Inc., Bethlehem, Pennsylvania, USA

M. Urteaga, W. Ha, J. Bergman, M. J. Choe, and B. Brar
Teledyne Scientific Company, Thousand Oaks, California, USA

M. T. Bulsara and E. A. Fitzgerald
Department of Materials Science and Engineering, Massachusetts Institute of Technology
Cambridge, Massachusetts, USA

D. Smith, D. Clark and R. Thompson
Raytheon Systems Limited, Glenrothes, Fife, United Kingdom

C. Drazek and N. Daval
SOITEC, Bernin, France

L. Benaissa and E. Augendre
CEA-LETI, MINATEC, Grenoble, France

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Abstract

The growth, fabrication, and integration of IIIV heterojunction bipolar transistors (HBTs) with Si CMOS on SOLES (Silicon-on-Lattice Engineered Substrate) has been demonstrated with first pass, first wafer success. DC and RF Measurements of HBTs on SOLES, and a differential amplifier comprised of HBTs integrated with Si CMOS are presented.

INTRODUCTION

Compound semiconductor device integration with silicon CMOS devices is becoming increasingly attractive as CMOS devices approach scaling limits, and as system on a chip applications emerge. The performance and utility of traditional approaches to heterogeneous integration of IIIVs with CMOS, such as wire bonded or flip chip multi-chip assemblies (Fig 1, left), are constrained by the variability and losses of the interconnects and by the placement of III-V device die relative to CMOS transistors. A more attractive approach is the direct integration of CMOS and III-V devices on a common silicon substrate (Fig 1, right).

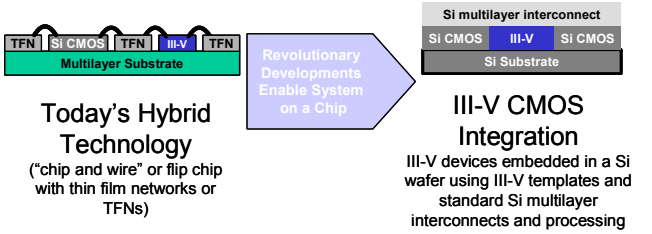
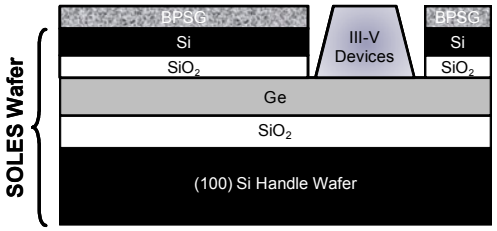


Fig. 1 Traditional hybrid assembly (left) and direct monolithic integration of III-V and CMOS on SOLES substrate (right)

Our direct integration approach is based on a unique silicon substrate which is similar to a standard SOI wafer. The SOLES (Silicon-on-Lattice Engineered Substrate) contains a buried III-V Ge template layer that enables the direct growth of high quality III-V epitaxial material in windows directly on the silicon substrate (Figure 2 top). Figure 2 (bottom) shows an example of a IIII-V epitaxial material grown in a window on the SOLES wafers.



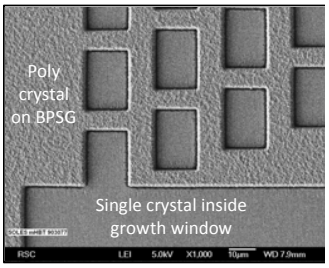


Fig. 2 Schematic (top) and SEM image (bottom) of III-V device material grown in windows on SOLES

With optimized growth conditions, low dislocation density (<10^7) material with good surface morphology (surface roughness < 1nm as measured by AFM) and well defined X-ray spectra are easily achieved. Since the III-V growth windows are lithographically defined as part of the CMOS fabrication process, the III-V epitaxial material can be grown selectively and arbitrarily across the substrate as required for the particular circuit or applications.

The DC and RF performance of InP HBTs fabricated on SOLES are comparable to HBTs grown on InP and GaAs substrates. Figure 3 shows the Gummel characteristics and small signal parameters of a 0.5 x 5 um^2 emitter HBT grown in a 15 x 15 um^2 window on a SOLES substrate. Gain (beta), f_t and f_{max} of 40, > 200GHz and > 200GHz, respectively are achieved.

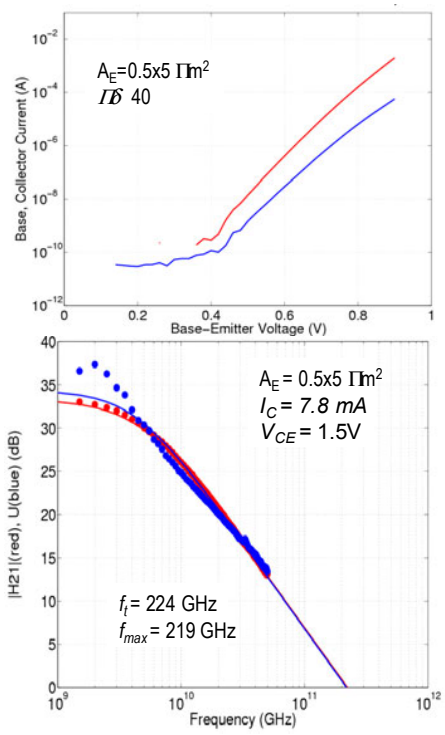


Fig. 3 Measured Gummel characteristics and RF gains of a 0.5x5 um^2 InP-HBT on SOLES substrate

Figure 4 shows a SEM image of a completed InP HBT in close proximity to a Si CMOS transistor. To facilitate the interconnecting of the III-V devices and CMOS transistors, the thickness of the III-V epitaxial layers and depth of the windows are optimized such that the III-V devices and CMOS transistors are planar. With this truly planar approach, interconnect lengths (III-V – CMOS separation) as small 2.5 um have been demonstrated. Using this approach we successfully fabricated differential amplifiers. Figure 5 shows optical micrographs of the completed differential amplifier core (top) and a differential amplifier with a bias circuit and all HBT output buffer (bottom).

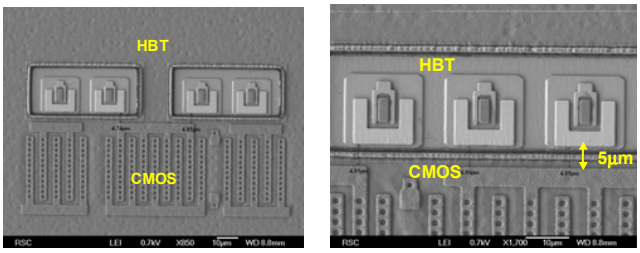
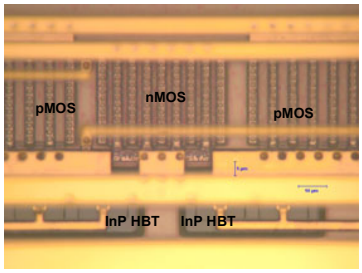
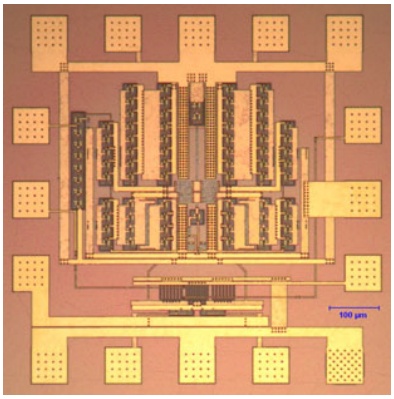


Fig. 4 SEM image of a completed InP HBT in close proximity to a Si CMOS transistor



Diff Amp core



Diff amp with output buffer and bias circuit

Fig. 5 Picture of the completed differential amplifier core of figure 4 (top) is shown, as well as a picture of the entire integrated circuit with output buffer (bottom).

Differential amplifier unity-gain bandwidth and low frequency gain measurements were performed using a 4-port vector network analyzer (Agilent PNA). Measurements were

made over a frequency range of 1MHz-20 GHz using on-wafer differential GSGSG probes. A probe-tip SOLT calibration was performed using a commercially available calibration substrate.

High frequency S parameter measurements of the differential amplifier output buffer circuit and the differential amplifier output buffer core chain were used to determine the unity gain cut off frequency (Figure 6) of the loaded differential amplifier. An extrapolated unity gain cut off frequency of > 25 GHz was achieved.

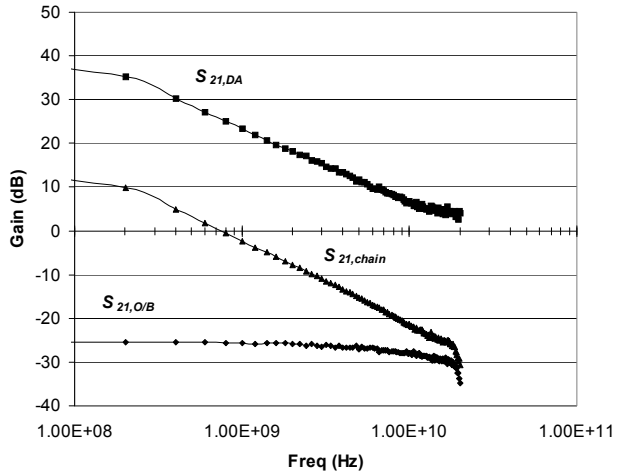


Fig. 6 Measured S_{21} of amplifier chain and output buffer test circuits at high frequencies. Scalar determination of diff amp gain is determined as $S_{21,DA}=S_{21,chain} - S_{21,O/B}$. Core diff amp utilized 3-2x5um^2 HBT in each diff amp branch with 6-finger 2um PMOS devices. I_{ss} = 10mA, V_{ss} = -6V.

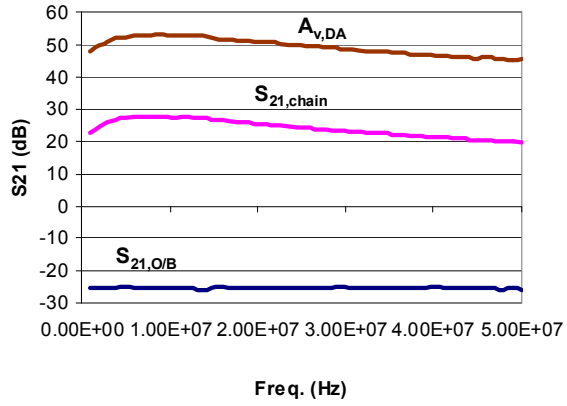


Fig. 7 Measured S_{21} of amplifier chain and output buffer test circuits at low frequencies. Low frequency gain $A_{V,DA}$ is given by $A_{V,DA}=S_{21,chain} - S_{21,O/B}$. Core diff amp utilized 3-2x5um^2 HBT in each diff amp branch with 6-finger 2um PMOS devices. I_{ss} = 10mA, V_{ss} - -6V.

For the same differential amplifier a low frequency gain (1-50MHz) 53.16 dB or 455V/V was measured (Figure 7). For this differential amplifier a DC gain-unity gain bandwidth product of >1.1x104 V/V-GHz is achieved.

We note that the low frequency gain is limited by the finite input impedance of the output buffer circuit. Simulations with the core only test circuit show a voltage gain that is ~3x higher than that of the loaded amplifier design.

To improve our DC gain in the future, a second iteration output buffer with a greater input impedance has been designed. This redesign should also allow the bandwidth of the buffer to be increased while reducing the power consumption (~40% lower). The bandwidth of new the design should increase from 13 GHz to 30GHz.

CONCLUSIONS

While the results presented here are for InP HBTs directly integrated onto the silicon substrate, the approach is equally applicable to other III-V electronic and opto-electronic (photodiodes, VCSELs) devices and opens the door to a new class of highly integrated, high performance, mixed signal circuits.

ACKNOWLEDGEMENTS

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ACRONYMS

HBT: Heterojunction Bipolar Transistor
SOLES: Silicon On Lattice Engineered Substrates