Technology for Dense Heterogeneous Integration of InP HBTs and CMOS

Y. Royter, P.R. Patterson, J.C. Li, K.R. Elliott, T. Hussain, M.F. Boag-O'Brien, J.R. Duvall, M.C. Montes, D.A. Hitko, M. Sokolich, D.H. Chow and P.D. Brewer

HRL Laboratories LLC,
Malibu, CA, 90265, USA;
Phone: (310) 317-5548; Email: yroyter@hrl.com

Abstract

For the first time, technology capable of wafer-scale device-level integration of InP HBTs and CMOS has been developed. With this technology full simultaneous utilization of III-V device speed and CMOS circuit complexity is possible. Simple ICs and test structures have been fabricated, showing no significant CMOS or HBT degradation and high heterogeneous interconnect yield. Resulting circuits maintain maximum CMOS integration density and HBT performance, while keeping the heterogeneous interconnect length below 5μm.

INTRODUCTION

III-V compound semiconductor device performance still greatly surpasses that of their Si counterparts, but CMOS has orders of magnitude higher level of integration and low power dissipation. Device-level integration of compound semiconductor (CS) devices with CMOS would enable a new class of high-performance high-functionality ICs [1] at a cost similar to CS ICs alone. For such heterogeneous ICs, InP DHBT technology is particularly suited due to the high device performance [2], high IC speed at low power [3], and circuit compactness as illustrated in Figure 1. The heterogeneous integration approach can use the latest CMOS technology, where as a monolithically integrated technology, such as SiGe Bi-CMOS, lags in the CMOS technology node and incorporation of the state-of-the-art SiGe HBTs is impeded by small market size relative to the development cost. In this work, we demonstrate wafer-scale device-level heterogeneous integration (HI) of 250nm, 300GHz f_T/f_{MAX} InP DHBT technology with IBM's 130nm RF-CMOS (CMRF8SF) technology.

PROCESS TECHNOLOGY

For this technology, InP DHBT epitaxial layers are bonded to the top interconnect layer of a CMOS wafer, which are then processed into HBTs and interconnected with the CMOS [7]. This process is illustrated in Figure 2 and images of the wafer at different stages are shown on Figure 3. The CMOS interconnect process is terminated at the last planar interconnect layer with only a thin dielectric layer on top of the copper. This surface is planar enough for wafer bonding to enable epitaxial transfer. The 200mm CMOS wafers are then cut into four 3inch wafers so that they can be further processed in our HBT line. Standard DHBT epitaxial layers are grown with the emitter side up on an InP substrate with thin etch stop layers inserted between the subcollector and the substrate. The DHBT wafer is then wafer bonded to a temporary Si handle wafer. The InP growth substrate is removed by wet etching, stopping on the etch stop layers. An Al heat spreader layer is then deposited on the subcollector. The epitaxial layers are then permanently bonded to the top CMOS surface using BCB adhesive layer [4]. The permanent bond can be a full-wafer wafer bond. However, die bonding was developed to allow the use of different size InP growth substrate and the substrate on which the HBT process is carried out. Thus, the HBT process can be carried out on the full size CMOS wafer. After the permanent bonding, the handle is removed, completing the epitaxial transfer process. The epitaxial transfer process consists of two bonding steps to ensure optimal epitaxial growth and device layout, which is with the emitter up in both cases.

After the epitaxial transfer, the InP HBT process is carried out. The CMOS wafer contains the alignment marks needed for the HBT processing. InP DHBT fabrication process on top of CMOS is similar to the standard process [5]. Alignment accuracy to the CMOS and between the HBT layers is limited by the stepper and is equal to our standard HBT process. Despite increased overall topography, critical dimension control for both electron beam and optical lithography is maintained. This alignment strategy enables dense and intimate device-level integration with <5μm heterogeneous interconnect length. After the HBT is fabricated, the heat spreader and the adhesion layers are patterned. The HBT and CMOS are finally interconnected through HI vias which connect the HBT interconnect metal to the top CMOS Cu interconnect layer. In addition to electrical vias, thermal vias that connect the heat spreader of each HBT to the Si substrate are also fabricated. Only one post-CMOS interconnection layer is used. All other interconnect layers as well as resistors and capacitors are fabricated as part the CMOS interconnect process.

RESULTS

To verify that the IBM CMOS devices are unaffected by the heterogeneous integration process, performance of the CMOS test devices that have gone through only IBM process and the ones that also went through the heterogeneous integration were compared. The IV characteristics of various IBM CMRF8SF library devices from HRL heterogeneously integrated wafers showed no signs of device degradation when compared to control IBM CMOS wafers. Figure 4

shows the typical transfer characteristics of a 1.5V thin-oxide, triple well NFET sampled from an HRL fabricated HI wafer and an IBM fabricated control CMOS wafer.

The HI HBTs performance was on par with our standard 250nm HBTs. For an A_E=0.25x4μm^2 InP DHBT, Figure 5(top) shows the forward Gummel characteristics and a DC current gain (β_f) >30; Figure 5 (bottom) shows common emitter IV characteristics and low output conductance; and Figure 6 shows f_T values >350GHz. Thermal resistance of the HBTs with thermal vias was determined by measuring the V_{BE} shift as a function of dissipated power at various ambient temperatures. Thermal resistance values as low as 13.0 °C/mW were obtained.

In order to assess the yield and resistive loss of the HI via, a 1000 unit long chain of the nominal 1.0x1.0μm^2 HI vias at a pitch of 5μm were electrically tested. Figure 7 shows the average HI via resistance is <400mΩ across the majority of the 3inch diameter wafer.

Technology robustness was assessed by comparing differential amplifier performance before and after wafer temperature cycling in an inert gas ambient. The temperature was cycled from -55°C to +85°C with 10 min dwell time at extremes. Comparison of slew rate and DC Gain x Unity-Gain-Bandwidth figures of merit before and after 100 thermal cycles (not under bias) is shown on Figure 8. This data indicates that our process produces robust devices and circuits.

Using the above technology, differential amplifier ICs [6] and DC and RF test structures were fabricated. The differential amplifier shown on Figure 9 demonstrated gain bandwidth product of 40-130 GHz, low frequency gain of >48dB, and a DC Gain x Unity-Gain-Bandwidth figure of merit of 1.6x10^4 GHz . The use of InP DHBTs supports a 6.9 V differential output swing with 0.4V differential input. A slew rate of 4.4x10^4 V/μs is achieved with as low as 40mW dissipated power. Presence of CMOS enabled the use of novel on-chip buffer circuits to facilitate the on-wafer characterization of these amplifiers. As can be seen from the amplifier schematic, intimate device layer heterogeneous integration had to be achieved for its realization.

Conclusions

Novel wafer-scale device-level heterogeneous integration technology is demonstrated. Dense HI integration without device degradation enables robust ICs that maintain both CS performance and CMOS functionality. This technology is applicable to any generation CMOS and HBTs, as well as other CS devices. CS device integration with CMOS could accelerate its maturity and utilization.

Acknowledgements

This work was supported in part by DARPA (Dr. Mark Rosker, PM) through AFRL (Dr. Gregory Creech) contract FA8650-07-C-7714 (CoSMOS).

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Technology	Speed	Power	TX Count	Market Driver	Pros/ Cons
InP DHBT	High	Mod	<10^4	Defense	BJT only, functionality limited
CMOS	Mod	Low	>10^9	Commercial	No precision fast device, low drive
SiGe HBT	Mod	Mod	<10^6	Commercial Defense	Lags latest CMOS
CoSMOS	High	Low	<10^4 / >10^9	Commercial Defense	Fastest CMOS and HBTs

Figure 1. Comparison of transistor speed, transistor count, power dissipation and target market of various technologies. HRL's CoSMOS heterogeneous integration technology can combine advantages of all these technologies for many circuit applications.

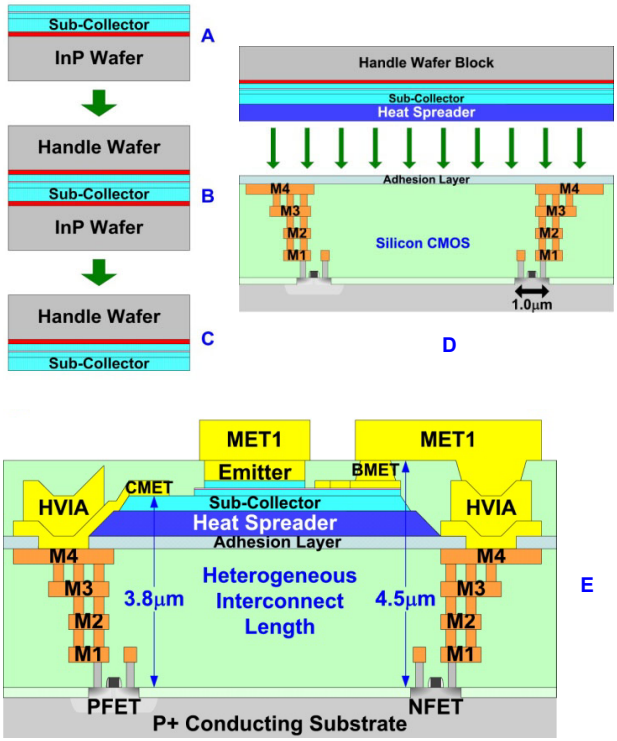

Figure 2. Schematic representation of heterogeneous integration process consisting of a) HBT epitaxial growth, b) temporary wafer bonding to a handle wafer, c) growth substrate removal, d) permanent bonding to CMOS after heat spreader deposition, and e) HBT fabrication and heterogeneous integration.

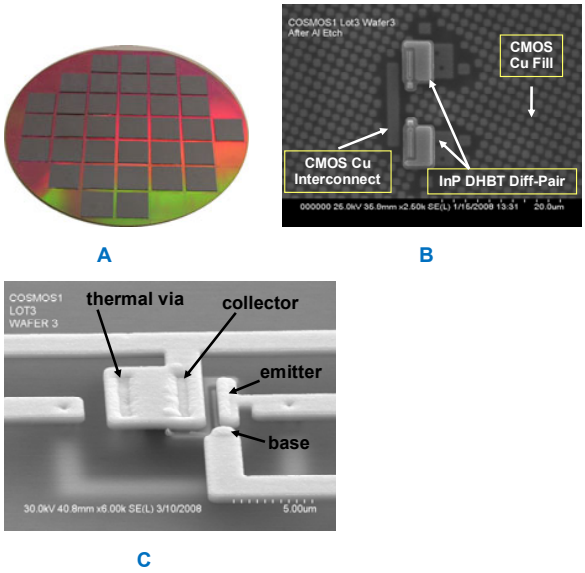

Figure 3. a) A photograph of an die bonded wafer at step E of Figure 2, b) an SEM micrograph HI integrated HBT before final interconnection, and c) an SEM micrograph of an HBT at the end of the process.

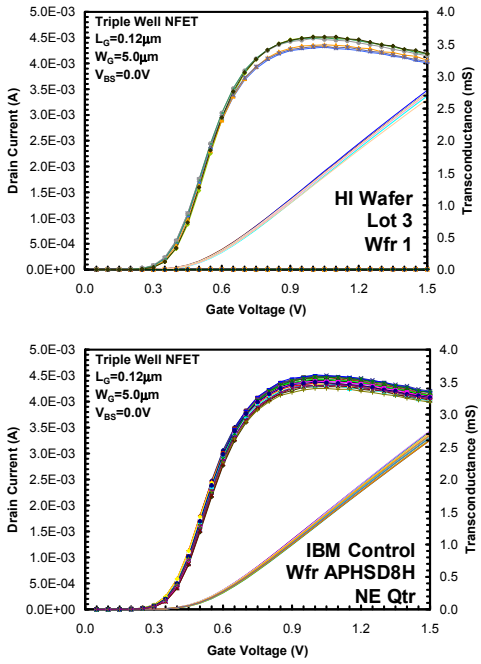

Figure 4. Transfer IV characteristics and associated transconductance, gm, from a 1.5V thin-oxide, triple-well NFET (LG=120nm, WG=5.0µm) bias at a VDS=1.5V and VBS=0.0V. A sparse sampling of 10 devices from a single HI wafer (top) and 22 devices from a quarter of the IBM control CMOS wafer (bottom) are shown.

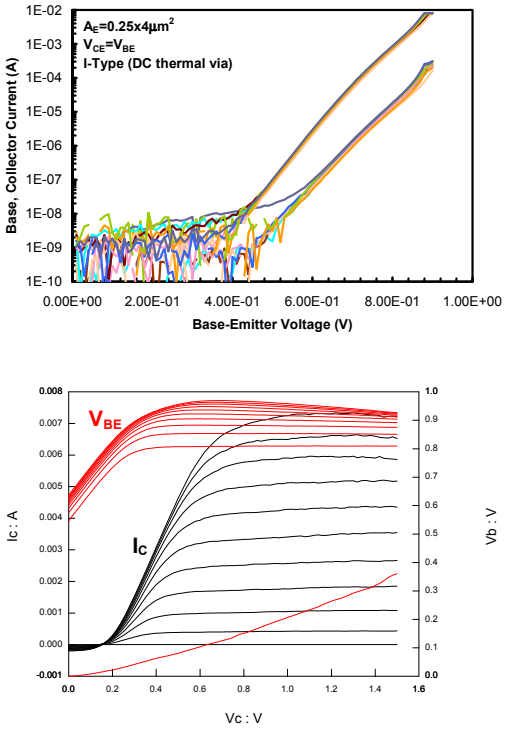

Figure 5. DC characteristics of an A_E=0.25x4.0µm^2 InP DHBT bonded onto CMOS: (top) forward Gummel with DC current gain (β_f) >30 while being driven at an I_C=10mA/µm^2 and a V_{CE}=V_{BE}; (bottom) common emitter IV and corresponding V_{BE} with I_B=0 to 200µA in 20µA steps.

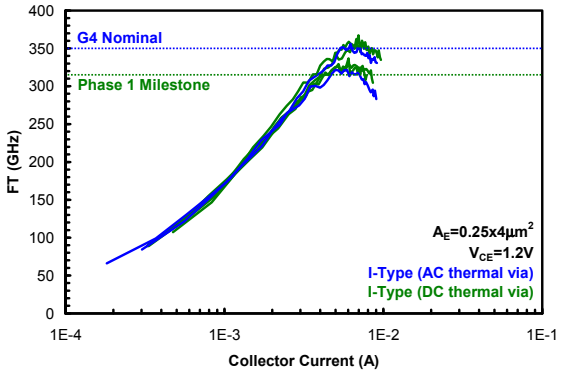

Figure 6. The f_T and f_{MAX} dependence with I_C of an A_E=0.25x4.0µm^2 InP DHBT while being driven by a forced I_B and fixed V_{CE}=0.8, 1.0, and 1.2V.

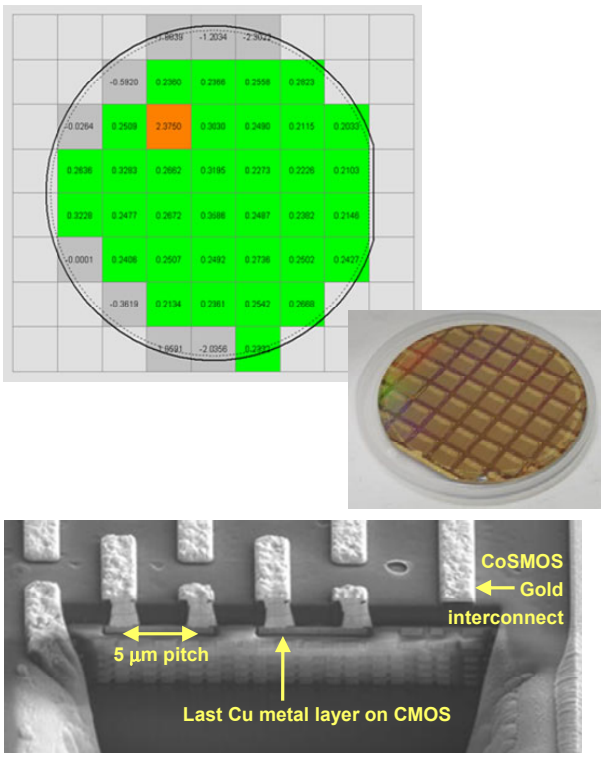

Figure 7. Wafer map showing the unit resistance in ohms of a 1000 unit long heterogeneous interconnect via chain with a 5µm pitch and 1.0x1.0µm^2 via size. Fully processed wafer and a cross sectional SEM of the via chain are also shown.

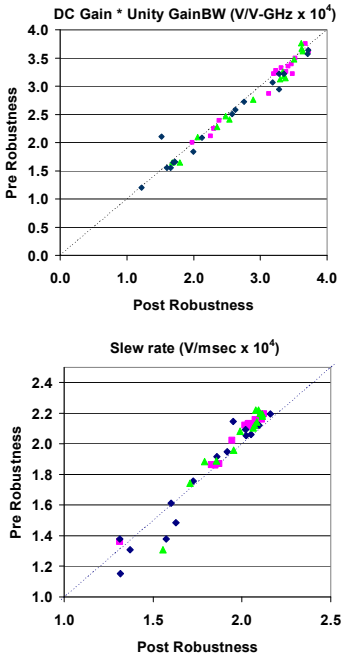

Figure 8. HI differential amplifier slew rate (bottom) and DC gain x unity gain bandwidth (top) comparison before and after 100 of -55°C to +85°C temperature cycles, indicating that the HI ICs are robust.

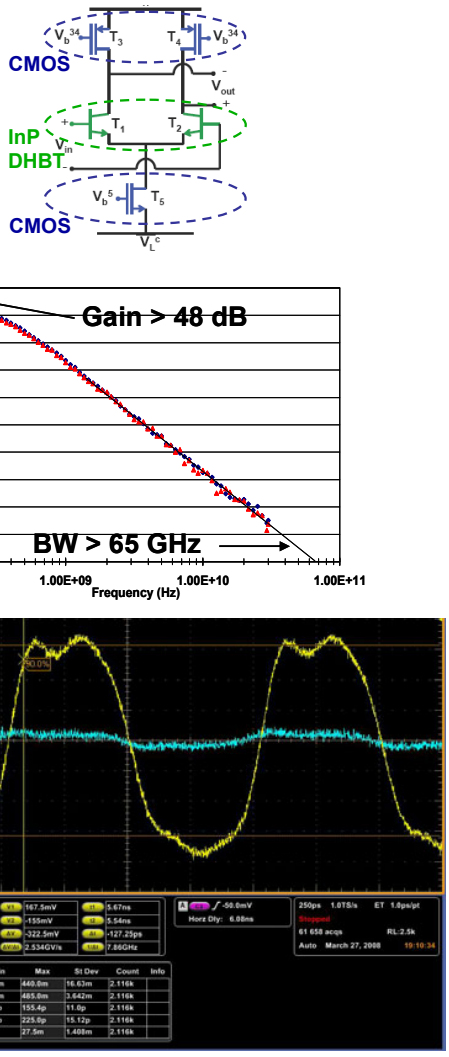

Figure 9. Heterogeneously integrated differential amplifier circuit schematic (top), measured gain versus frequency (middle) and digital oscilloscope capture of the measured large signal output swing (bottom). Low frequency gains of 48 dB were achieved simultaneously with a unity gain bandwidth >65 GHz. A 10-90% slew rate of 4.4x10^4 V/µs is observed with a 6.9V differential output voltage swing and a 0.4V differential input voltage swing.