GaN Power Switching Devices for Automotive Applications

Tsutomu Uesugi and Tetsu Kachi

Toyota central R&D Laboratories, Inc. Nagakute-cho, Aichi, 480-1192 Japan
E-mail: uesugi@mosk.tytlabs.co.jp,

Keywords: GaN, power devices, vertical structure, trench MOSFET

Abstract

It is widely recognized that Hybrid Vehicles (HVs) are suitable for solving problems of energy saving and reduction of CO_2 emission. For the future system, higher performance power devices superior to Si-IGBT, which is used for present HVs, are strongly required. GaN is the promising material for post Si power devices. We are developing GaN power switching devices. For high power switching devices, two types of vertical device structure have been developed. One is similar to double diffused MOSFET of Si. The other type is U-shape trench gate MOSFET. Both types of the power device have now insufficient performances for the applications. However, GaN has shown the potential as the post Si materials of high power devices.

1. INTRODUCTION

Development and improvement of hybrid vehicles (HVs), electric vehicles (EVs) and fuel cell hybrid vehicles (FCHVs) are now widely recognized as one of solutions of the CO_2 problem of the earth scale, the exhaust gas problem of urban areas and the fuel consumption problem. These vehicles need high electric power inverters to drive high power motors. In the present time, Si insulated gate bipolar transistors (Si-IGBTs) are used in the inverters of HVs. However, Si devices have a limitation of performances due to their material limits. Devices with higher performances, which are, for example, higher operating temperature and lower on resistance, are strongly required for future vehicles. In this paper, we discuss automotive applications, especially hybrid vehicles, of power devices and the recent development of GaN power devices.

2. POWER DEVICES FOR HYBRID VEHICLES

Figure1 shows the relationship between the motor power of Toyota's HVs and power source voltages of these systems. The first generation Prius was on market in 1997. Through the inverter of this hybrid system, the battery voltage of 277V was directly connected to the motor. The second Prius has been on the market since 2003. In its HV system, the battery voltage of 202V is raised to a power source voltage 500V by a voltage booster and then supplied to the motor through the inverter. New HVs need high motor power with high power source voltage as shown in Fig. 1. The breakdown voltage of devices used in these inverters is about 1kV. Higher breakdown voltage of devices used in the inverters is required in the future due to higher motor power and protection against surge voltage. Moreover, low on resistance of the power devices and high temperature operation above 200°C are also required to simplify the cooling system of the inverter. Therefore, the requirements for power devices are followings. The breakdown voltage

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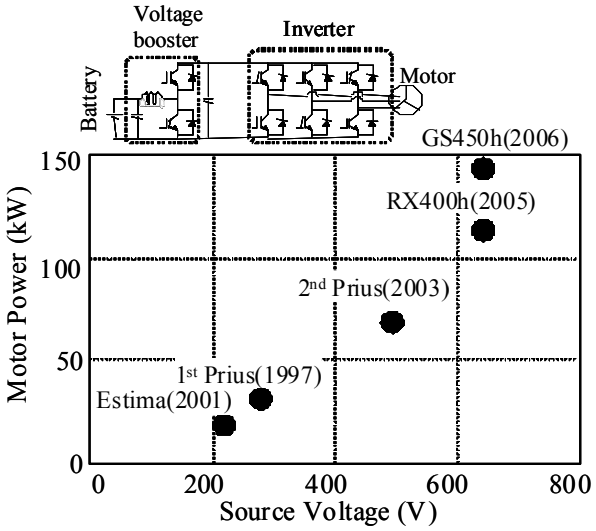


Fig.1 Power source voltage vs. motor power of TOYOTA's HVs.

3. VERTICAL STRUCTURE DEVICES

GaN has material properties proper for power switching devices such as wide band-gap, high break down electric field, high saturation velocity. The potential of GaN for power devices has been recently widely recognized and developments of AlGaN/GaN field-effect transistors (FETs) for high power switching applications have progressed. Most

of these devices have been lateral device structure because the structure was based on the high frequency devices. The lateral structure is suitable for a low power switching device. However, for over 20~30 kW power, vertical device structure is more suitable. The vertical structure has following merits, for example, small chip size, easy wiring, high breakdown voltage. Especially, current collapse-free operation, which is a problem for the lateral AlGaN/GaN structure, can be expected because the current flows in the balk GaN, which is not affected by surface states. However, the vertical device has not developed until recently because of the lack of high quality free standing GaN substrates. Recently, 2 inch GaN substrates have become supplied from several suppliers. We started the development of vertical power switching devices using GaN substrates several years ago. We have been developing the vertical structure GaN devices, which were two types of the vertical structure. One is AlGaN/GaN HFET, of which structure is similar to double diffused MOSFET and the other is trench gate MOSFET.

3. 1 VERTICAL AlGaN/GaN HFET

One type of our developments is similar to a double diffused metal oxide semiconductor field effect transistor (DMOSFET). Figure 2 shows schematic cross-sectional view of the developed device structure [1]. The device was formed on an n-type GaN substrate. The current flows vertically from the drain to the source. The gate channel was the AlGaN/GaN interface and the gate was an insulated gate using SiO_2 for the insulator. The Mg-doped p-GaN layer functions as a current blocking layer and the current flows through the aperture made at the center of the blocking layer. The fabrication processes are as follows. Epitaxial layers for the device structure were made by metal organic chemical vapor deposition method (MOCVD). A 3 µm-thick n-GaN layer (Si:1x10^{16} cm^{-3}), a 0.1 µm-thick p-GaN layer (Mg:3x$10^{19}$$cm^{-3}$), a 10 nm AlN layer, and a 50 nm i-GaN layer were grown on a c-plane n-type GaN substrate. by metal organic vapor phase deposition (MOCVD). The center of the i-GaN/AlN/p-GaN layers was etched by inductively coupled plasma (ICP) dry etching with Cl_2 gas using an SiO_2 mask. The etching depth was about 0.28 mm. After the removal of the mask, a 0.3 µm n-GaN layer (Si: 1x10^{16} cm^{-3}) and a 15nm $Al_xGa_{1-x}N$ (x~0:25) layer were grown. During

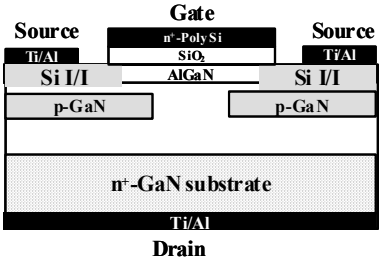


Fig. 2 Cross sectional view of the vertical insulated gate AlGaN/GaN HFET.

this re-growth process, the AlN layer suppressed the upward diffusion of the Mg atoms in the p-GaN layer as well as the mass transport from the surface to the aperture region. This re-growth process covered in the trench. The source regions were formed by Si ion implantation at an acceleration energy of 40 keV with a dose of 3 x10^{15} cm^{-2} and the activation annealing at 1000 ºC for 20 min with an SiO^2 encapsulated layer. We obtained a specific contact resistance Rc of about 8x10^{-5} Ω·cm^2 with a circular transmission line method (c-TLM). The isolation region was formed by N^{2+} ion implantation at the acceleration energy of 30 keV with a dose of 5x$10^{14}$$cm^{-2}$. A 50 nm high-temperature SiO_2 (HTO) layer as a gate insulator was deposited by low-pressure chemical vapor deposition (LPCVD). It was reported that the density of interface states of HTO/GaN was as low as 2x10^{11} $eV^{-1}cm^{-2}$ [2]. A 250 nm phosphorous doped polycrystalline silicon (poly-Si) film as a gate electrode was deposited by LPCVD, followed by the activation annealing at 850ºC for 20 min in a nitrogen ambient. At the same time, the Mg in the p-GaN layer was also activated. The poly-Si gate electrode was defined by dry etching. A 500 nm SiO_2 interlayer was deposited by plasma CVD and the contact holes were formed by dry etching. Finally, the source and the drain electrodes Ti (20 nm)/Al (1 µm) were formed by electron beam (e-beam) evaporation.

The measured HFET had two striped gate electrodes, a gate width of 40 µmx2, a gate length of 2 µm, an aperture width of 3 µm, and an active area of 40x51 µm2. Figure 3 shows I_D–V_{DS} characteristics at V_{GS} = 0, -5, -10 and -15 V. The threshold voltage (V_{th}) was -16V. No current offset was observed at V_{DS} = 0 V. This indicates that there were no barrier layers in the contact region as well as in the aperture region. We calculated the specific on-resistance (R_{sp}) from the linear region around V_{GS} = 0V. The calculated R_{sp} was 2.6 mΩ·cm^2. On the other hand, the breakdown voltage was less than 50V, which was limited by the breakdown of the gate insulator (HTO). In this device structure, p-GaN layer was in floating state. Therefore, drain voltage was applied to

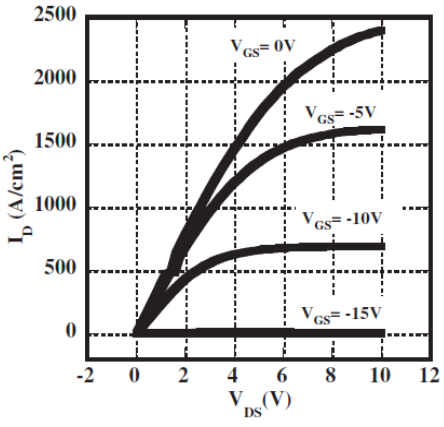


Fig.3 I_D–V_{DS} characteristics of the vertical insulate gate AlGaN/GaN HFET

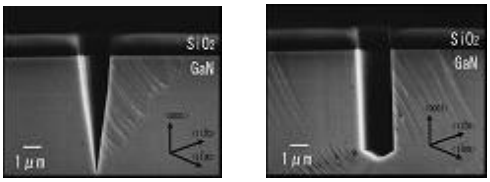
the gate insulator. To obtain higher breakdown voltage, the structure has to be improved. For example, an ohmic contact

on the p-GaN layer is necessary and thicker p-GaN layer and n^--GaN drift layer are also needed for higher breakdown voltage.

3.2 TRENCH GATE MOSFET

Trench gate structure has a capability of very short cell pitch on a device. It results in low on resistance. However, it is difficult to fabricate the smooth surface on the trench sidewalls for a gate channel. We have developed novel fabrication process of gate trenches.

Trenches were first formed with dry etching. Figures 4(a) shows scanning electron microscope (SEM) images of the trench after the dry etching along the [11-20] direction on a free standing (0001) plane GaN substrate. The dry etching for the trench has made with inductively coupled plasma (ICP) etching using Cl_2 and BCl_3 gases. The trench width at the surface was 1.5 μm. The etched trenches showed the V-groove and rough side walls as shown in Fig. 4(a). The dry etched surfaces are not suitable for a gate channel because of the surface roughness and the damage by ion bombardments. Therefore, post-treatment of the surfaces is needed for smoothing the surface and removing the damage. Wet etching is desirable for the post-treatment. We have developed the novel wet etching method using tetra-methyl-ammonium hydride (TMAH). TMAH is widely used as a photoresist developer in the photolithography process and also used as an anisotropic etchant of silicon. We have tried to etch GaN using TMAH and found that any planes of GaN except for the (0001) plane were etched by TMAH. Figure 4(b) shows the images of the trenches after the wet etching of the V-groove trenches. The wet etching was performed at 85ºC for 1 h with TMAH of the concentration of 25%. The V shape turned to U shape of which tapered angle of the side walls was 90º. The side walls were smooth m-planes. This result shows that the etching rate for a (1-100) plane is lower than other planes. The trench structure is appropriate for the trench gate of MOSFET.



(a) (b)

Fig.4 SEM image of the (a) dry etched trench and (b) followed by TMAH wet etching. TMAH wet etching is effective for obtaining the m-plane surface.

3.2.1 ACCUMLATION MODE OPERATION

We have fabricated the U-shape trench gate MOSFET (UMOSFET) using the developed etching process on a (0001) plane n-type GaN substrate to examine the characteristic of the channel on the (1-100) plane. Figure 5 shows the cross-sectional photograph of the UMOSFET. A 2μm undoped-GaN and 0.5μm n-type GaN (Si: $3x10^{18}$ cm^{-3}) was grown on the substrate by MOCVD. The U-shape gate trench was produced by the dry etching and the wet etching as mentioned above. The 1.2 μm width gate trench pattern was formed along the [11-20] direction. A 50 nm HTO film as a gate insulator and 1 μm phosphorous doped poly-silicon film as a gate electrode were deposited by LPCVD. The gate channels were formed on the (1-100) trench side walls. After definition of the gate, 1 μm SiO_2 was deposited as interlayer dielectric layer. Finally, after contact holes were fabricated 500 nm Al layers as the source and drain electrodes were deposited by electron beam evaporation. The UMOSFET has a channel length of 2μm and a channel width of 40 μm. The drain current-gate voltage characteristics (I_D-V_G) are shown in Fig.6. The measurements were made from room temperature to 300ºC. In this measurement, the drain voltage was 0.1V and the source voltage was 0V. The channel mobility was calculated from the maximum value of the transconductance. The calculated value of the channel mobility at room temperature was 117 $cm^2/V{\cdot}s$. This channel mobility is same order of magnitude of the reported MOS channel mobility on the c-plane. This indicates the potential of the etched surface for the channel.

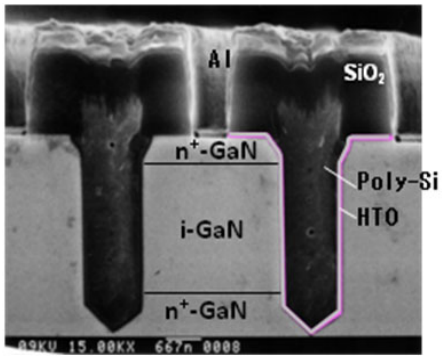


Fig.5. The cross-sectional photograph of the UMOSFET

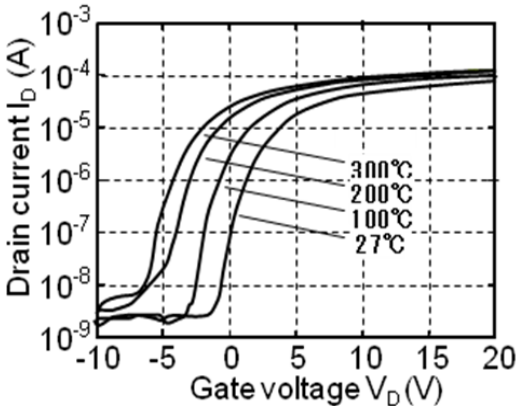


Fig.6 I_D-V_G characteristics of the UMSFET. The measurements were made from room temperature to 300 ºC.

The measured threshold voltages are all negative as shown in Fig.6 because undoped GaN layer is high resistive

n-type which lead to accumulation mode operations. Therefore, the positive threshold voltage will be obtained using p-type GaN as the channel layer.

3.2.2 ENHANCEMENT MODE OPERATION

We have also fabricated the trench gate FET having a p-type GaN body layer as shown in Fig.7 [7]. In this case, SiN film was used as a gate insulator instead of SiO_2, because of its larger dielectric constant to obtain high breakdown voltage. Main fabrication processes are same as previous processes. A 6 µm thick n-type (Si: $2x10^{16}cm^{-3}$) GaN and 1 µm thick p-type GaN (Mg: $7x10^{18}cm^{-3}$) was grown on the n-type substrate. The source regions were formed by selective ion implantation at acceleration energy of 40 keV with a silicon dose of $3x10^{15}$ cm^{-2}. The activation anneal was performed at 950 ºC for 20 min in N_2. The U-shape gate trench was produced by the same method as mentioned above. The 1.2 µm width gate trench pattern was formed along the [11-20] direction. A 100 nm thick SiN film as a gate insulator and 1 µm phosphorous doped poly-silicon film as a gate electrode were deposited. The gate channels were formed on the (1-100) trench side walls. Finally, the source and drain electrodes were produced.

The typical I_D-V_G characteristics under drain to source voltage 0.1V are shown in Fig.8. The threshold voltage of 10 V was obtained. However, the V_{th} is lower than calculated value of 44V. The characterization of the trench sidewall surface is under investigation. The breakdown characteristics were also measured. The breakdown voltage was 180 V, which was highe than the gate insulator breakdown voltage. This indicates that the depletion layer extended under the insulator. However, the breakdown occurred at the gate insulator film. For higher breakdown voltage, the structure of relaxing the electric field crowding around the trench is needed.

Our results show that the trench gate structure, which is widely used for Si based power transistors, can be applied for GaN based transistors.

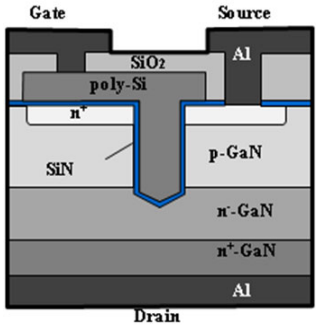


Fig.7 The schematic cross-sectional view of the UMISFET.

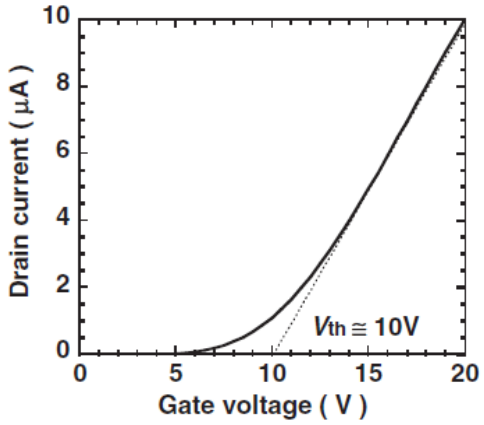


Fig.8 Typical I_D-V_G characteristics under drain voltage of 0.1V.

4. CONCLUSIONS

Two types of the vertical GaN power devices developed by our works have been introduced. Transistor operations have been accomplished for both types. However, there are many subjects to be developed. Vertical devices of GaN are now only on the start line of the progress. On-resistance, breakdown voltage, current capacity and so on are yet far from the expected properties. The fabrication processes are not yet optimized and determined. Novel fabrication technology and device structure needs to be developed for the vertical devices.

History of GaN power devices is shorter than that of Si and SiC power devices. Nevertheless, performance of the GaN power device has been progressing rapidly. To overtake existing power devices, total progress of technologies for GaN power devices, such as GaN substrates, processing and device design, has to be accelerated.

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