Challenges as an Independent GaAs Foundry– A Manufacturing Perspective

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Abstract

In this paper, we discuss the challenges an independently running foundry is facing from the manufacturing perspective. Some of these challenges are common in the CMOS foundry business but get amplified by the fact that compound semiconductor has a much smaller scale of economy. Other issues are unique to our industry.

INTRODUCTION

What a foundry puts into production must go through the development stage. What we mean by "input end" here refers to the challenges we have to "bear" from the development stage. In the traditional semiconductor vertically integrated model (IDM), the firm must possess the capability from product integration, circuit design, semiconductor manufacturing, component packaging, all the way to final product verification. To bridge all these different know-hows is the ultimate test for a successful IDM firm. Boundaries in between are never black and white. Quite often, one can find a particular packaging technology amplifying/canceling out some weaknesses associated with a semiconductor technology. The bottom line is adding all these technologies together; the final product works in the end market. It is not unusual a product is released only after a comprehensive set of tests to identify the design/process windows of various techniques which lead to consistent mass production.

CHALLENGES FROM THE INPUT END

Being an independently operating foundry, nevertheless, do not possess that visibility. The core competence of foundry mostly resides in the ability to manufacture semiconductors. Development talents are built around the capability to generate technology once a specification (always comes from product/circuit requirement) is decided. This goes beyond the domain knowhow of foundries. One can imagine it is really not that rare that a technology is built and released but few customers find it fit in well with their applications.

Working with key customers during technology development stage does alleviate the problem to a certain degree but does not fix it once and for all. One specification may fit the development partner perfectly but others still find a "tune up" is much desired as different designers have their own signatures. To accommodate as many customers as possible, technology revision does happen often. The drawbacks are twofold – production is facing constant change and manufacturing redundancy is reduced.

CHALLENGES AT MANUFACTURING STAGE

What semiconductor people refer to "scale of economy" usually means the utilization of their factories together with the lumped capacity wherein. From a cost/investment point of view, these are indeed important topics we should be concern about. Having said that, another layer should never be left out is manufacturing redundancy. Manufacturing redundancy is the number of tools that can be used for the same process. Equipment does go down for preventive maintenance and sometimes, unexpectedly' due to mechanic malfunction. For wafer lots get caught by such incidence, an extra penalty in cycle time is added upon. "Fortunate" wafer lots, not caught by any equipment downtime, are completed earlier while "unfortunate" lots take longer time to finish. This is commonly understood as production variability. Depending on the technology, our historic figure shows that number is somewhere between 3 ~ 8 days.

Adding on extra equipments effortlessly takes away production variability. This is easier said than done, though. Most of the equipments we have at WIN Semiconductors' 6" production facility are down converted from 8" tools designed for CMOS process. These pieces of equipment are designed with the highest throughput in mind. Unfortunately, it also means we, representing operation at much smaller scale, would only need one or two of these tools. Another equally important factor is the number of technologies/revisions a factory runs. In FAB A of WIN Semi, there are 15+ different flavors of technologies running in the shop floor at all times. Equipments are further spread over to support all the varieties.

Combining the humongous equipment throughput together with the variety of technologies, manufacturing

redundancy can be very thin for a GaAs foundry which is never a problem for Si foundry. Si foundries do mix products in the same manufacturing line but they do not mix processing technologies. This is largely due to the fact their economic scale can afford that. Unfortunately, it is for sure our fate utill the compound semiconductor industry grows by tenfold. Addressing this issue effectively is hence a key factor to be successful in this business.

LESSONS FROM THE CMOS INDUSTRY – THE ROLE OF SEMI STANDARD

The challenges we discuss above almost replicate what the Si industry has been through in 1960s and 1970s. Back at that time, there were over 2000 user specifications for Si wafers existed. Wafer manufacturing tools had to be readjusted continually from one order to the next, causing lost time and raising costs. In 1970, a significant event which later influenced the entire industry (especially, foundries) happened – the founding of SEMI Standard.

The impact of SEMI in general has two fronts. One centers around its industry roadmap published yearly. The roadmap lines up the entire industry from product application to verification/testing. Semiconductor developers know exactly what specification they need to achieve by what time. The existence of roadmap is in particular valuable to foundries as discussed earlier – where forward-looking capability is usually lacking.

The other impact of SEMI Standard is even more profound. It puts all material suppliers and equipment vendors under the same roof. Development resources are focused to tackle on critical problems rather than spread over to deal with customized tools and materials. The industry hence moves faster, draws more talents in and puts forward more applications to the market.

CONCLUSION

In summary, we discuss the different facets of challenges an independently operating GaAs foundry is facing. Among those, manufacturing redundancy is key. "Recycling" processing technologies in development work is the solution. Nonetheless, it would only be effective if a foundry can establish better application visibility. SEMI experience is then discussed to make a comparative analogy with the GaAs industry.

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