High Frequency Wafer Level Reliability Test Bench with Variable Load Impedance

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Abstract

This paper describes an on wafer reliability test set to stress transistors under RF conditions. The setup provides a thermo chuck and a mechanical tuner at the output of the transistor under test. With this configuration, transistor degradation due to the effects of different load lines can be determined. Initial results from tests done on GaAs pHEMTs and GaN HEMTs are presented.

INTRODUCTION

For the development of new technologies, and the modification of existing technologies in production lines, a method for fast reliability testing is important for promoting short feedback loops and quick process improvements [1][2]. To date, High Temperature Operating Live-tests (HTOL) at the wafer level were performed at UMS using stressing only under DC biasing conditions. Most often, however, transistors are used for power amplifier applications. In order to have wafer level test conditions more closely match these applications we have built-up a wafer level reliability test bench using an RF signal, a variable load impedance at the output of the Device Under Test (DUT) and a thermo chuck.

WAFER LEVEL RELIABILITY TEST BENCH

A schematic of the test bench is shown in Figure 1.

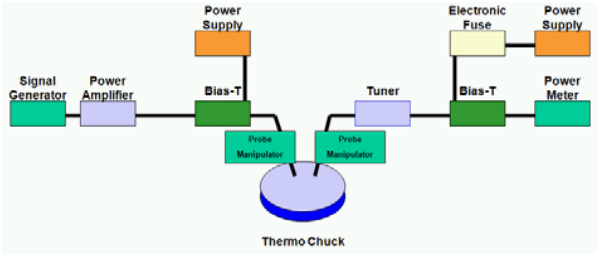

Figure 1: Schematic of test bench

The signal generator used (Agilent E8257) can provide frequencies up to 20GHz. To get sufficient power at the input of the DUT a power amplifier with an output power of 30dBm in a frequency range between 2GHz and 8GHz follows the signal generator. Additionally a TWT amplifier with Pout=40dBm in a frequency range between 8GHz and 18GHz is available. The devices being tested are connected by GSG-probes (125µm pitch) on both sides. The input port of the device sees an impedance of 50Ω. At the output side of the DUT a mechanical tuner is used to adjust the load impedance to the desired value. Due to the losses of the probe, connector and tuner the impedances seen at the output of the DUT cover a reflection range of $|\Gamma|<0.8$. The mechanical tuner is fixed to the manipulator (SUSS MicroTech PH250), so the impedance does not change by moving the probes. After the tuner, a 20dB attenuator is connected and the power is sensed by a power meter. To prevent damage on the probes after a short circuit on the DUT, and to better analyze the damaged device, an electronic fuse is used in the DC path at the output side of the DUT. The bias supplies provide an output voltage up to 100V. This is sufficient for stressing even GaN HFETs. The thermo chuck for the wafers provides temperatures up to Tcase=200°C. With a parameter analyzer (Keithley 4200) intermediate measurements can be performed. These measurements include drain and gate leakage current measurements, the basic transistor parameters like break down voltage and the gm-curve. A network analyzer (HP8720B) is used for adjusting and characterizing the tuner states. The software for this setup was developed in-house using HP-VEE. The program performs the power calibration, DC measurements for adjusting the biasing, power sweeps and the stress test. After starting the stress test by entering the bias condition and the input power level, the software program records the output power level, and the drain and gate current/voltage with a constant time delay.
Although the setup can handle frequencies up to 18GHz the preferred operation frequency is 2GHz. This simplifies the handling.

Besides this test bench a commercial load pull test bench using electronic tuners is available to characterize the devices and figure out appropriate load impedances for the different technologies. These impedances can be used for wafer level reliability test bench.

Before using the new test bench, comparative measurements were performed on both setups. The same transistor with the same bias conditions and load impedance was measured on both setups. These measurements showed low deviation <0.2dB between both setups, see Figure 2.

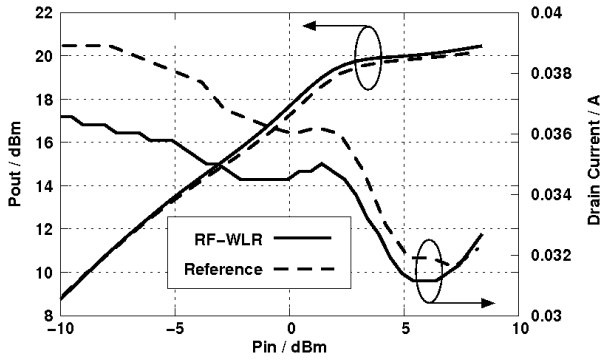

Figure 2: Comparison of the output power vs input power for the same transistor on the different test benches

Since the load impedances for the harmonics are not matched on both setups this can be a source of deviation in the measured results.

The setup up can handle all UMS technologies: MESFET, low noise pHEMT, power pHEMT, GaAs-HBTs and GaN HEMTs.

MEASUREMENTS ON GAN HEMTS

In a first experiment we assessed the power degradation of GaN HEMTs. Two transistors (2x400µm) from the same wafer were stressed at different drain voltages of Vds=30V and Vds=40V. The quiescent drain current for theses transistors was adjusted to 200mA but increased for the stress condition to 250mA and 266mA due to the increase of the input power level. The load impedance was determined on the separate load pull setup for optimum output power to be Rl=67Ω at 2GHz. The input power levels for the stress test are 20.4dBm and 20.9dBm which corresponds to a compression level of about 4dB. Both transistors were stressed for more than 160h at Tcase=150°C. The evolution of the output power level over time is shown in Figure 3.

The output power levels at 150°C are 3.8W/mm and 4.5W/mm respectively. The transistors stressed with Vds=30V and Vds=40V degrade after 170h ΔP=0.30dB and ΔP=0.43dB. For the transistor stressed at Vds=40V the gain versus input power before and after the stress test at Tcase=30°C is shown in Figure 4.

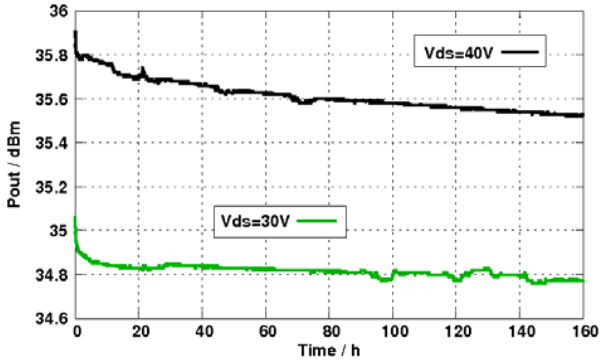

Figure 3: Power degradation of GaN HEMTs at Tcase=150°C for Vbds=40V and Vbds=30V

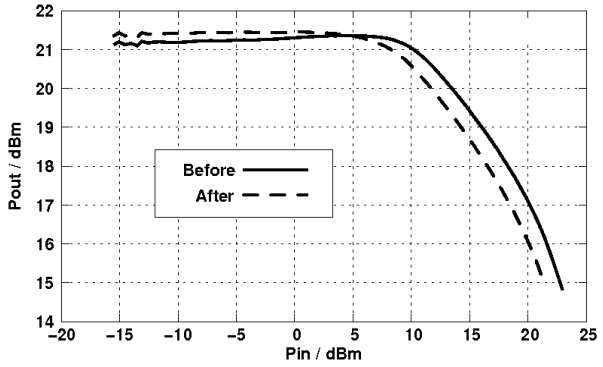

Figure 4: Gain vs input power level before and after the stress test for the transistor biased with Vds=40V

It can be seen that the linear gain for this transistor hardly changed. However, after the stress test the compression starts at a lower input power level. The power sweeps were performed for the same gate voltage. The early compression can be attributed to a reduced drain current after the stress, which was also measured.

MEASUREMENTS ON GAAS PHEMTS

For a newly developed GaAs pHEMT technology (Lg=150µm, Vbds=12V) a stress test with this test bench was performed in an early stage of the technology development. The transistor had a size of 8x75µm and was biased during the stress test with Vds=6V and Ids=160mA. This biasing corresponds to class A operation, therefore the drain current only slightly increased with increasing input power level. The input power level was 14dBm, which corresponds to more than 5dB compression. The chuck temperature was Tcase=150°C. The evolution of the output power level during the stress test is shown in Figure 5.

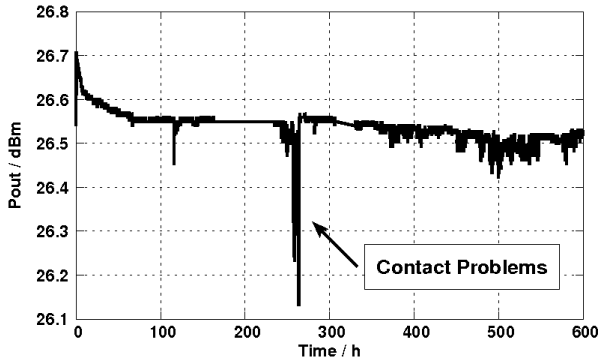

Figure 5: Power degradation of GaAs pHEMT at Tcase=150°C

This transistor showed a low degradation of just ΔP=0.2dB after 600h. Most of the degradation happened within the first 100h. For this transistor the linear gain degraded after the stress test at Tcase=30°C about 0.5dB. The power gain for a compression level above 2dB is nearly identical, see Figure 6.

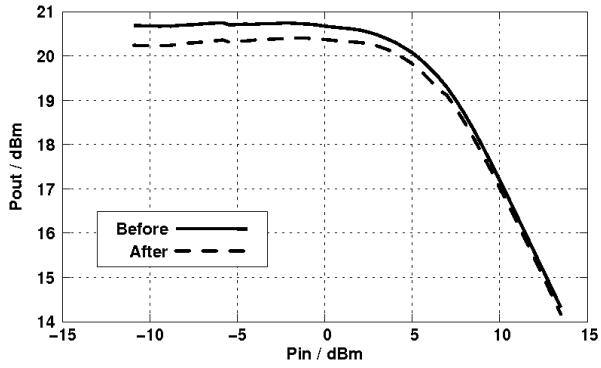

Figure 6: Gain vs input power before and after the stress test

The following experiments were performed on a different GaAs pHEMT technology (Lg=260nm, Vbds=18V) at Tcase=25°C. For these tests the load impedance was varied between 6Ω and 200Ω. The transistor used (8x75µm) was designed to match well for Rl=50Ω. For each test a new transistor was examined and for all tests the quiescent biasing (Vds=9V, Ids=90mA) and the input power level (12.2dBm) were fixed and correspond to 4dB compression for a load of Rl=50Ω.

Figure 7 shows the degradation in the output power level after 100h dependent on the load impedance. It can be clearly seen that the degradation increases significantly with decreasing load impedance. This is important information for the designer to avoid impedance levels where the device shows high degradation.

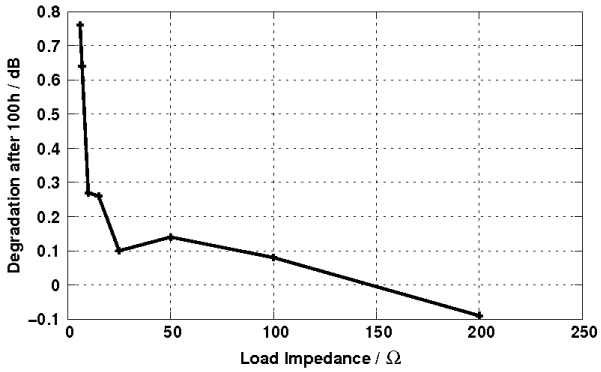

Figure 7: Degradation after 100h for different load impedances

When looking at the evolution of the output power level during a stress test the power level often increases during the first hours before decreasing. This is the reason for the negative degradation at a load impedance of 200Ω. Different reasons can be attributed to the increased degradation with decreasing load impedance. First the dissipated power in the device drastically increased with decreasing impedance. Figure 8 shows the efficiency versus the load impedance.

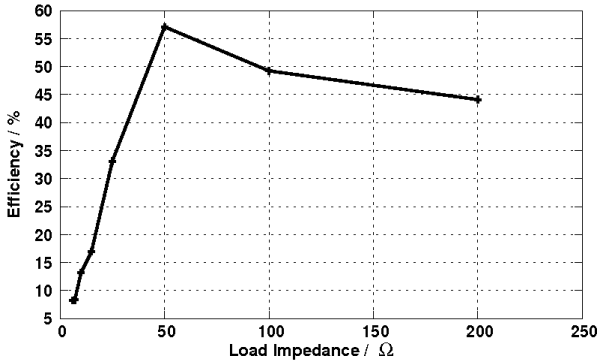

Figure 8: Efficiency vs load impedance

The efficiency at Rl=50Ω is highest with 57% and drops significantly with decreasing load impedance. Also the DC current level increases in with an RF-signal applied to the transistor with decreasing load impedance. So the transistors stressed with a low impedance see a higher temperature during the stress test. Due to the different load lines the transistors are operated in different regions. Using a low impedance the transistor is operated in a region with a high current and high voltage level. This region is prone to impact ionization, which is also a source of degradation.

COMPARISON OF DIFFERENT EPI SUPPLIERS

For the qualification of new Epi suppliers for a double recess technology (Vbds=12V, Lg=240nm) transistors processed on the different Epis were stressed. The devices have s size of 2x75µm and the test conditions are: quiescent

biasing Vds=6V Ids=40mA, Pin=6.6dBm and Rload=162Ω. The chuck temperature was Tcase=150°C. Figure 9 shows the power degradation versus time for the first 120h of our standard Epi and the two suppliers Q1 and Q2.

The degradation of all three different Epi suppliers is very low. It ranges from ΔP=0.03dB for our standard Epi supplier up to ΔP=0.08dB. Looking at the gm-curve recorded before and after the stress test the transistors processed on the Epi from supplier Q2 show a shift in the gate voltage of 0.1V, see Figure 10.

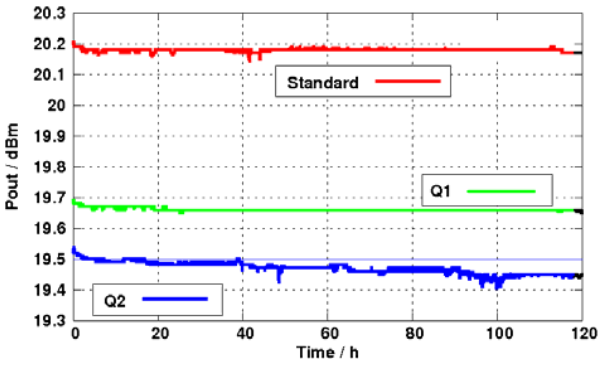

Figure 9: Power degradation of transistors processed on Epi layers from different suppliers

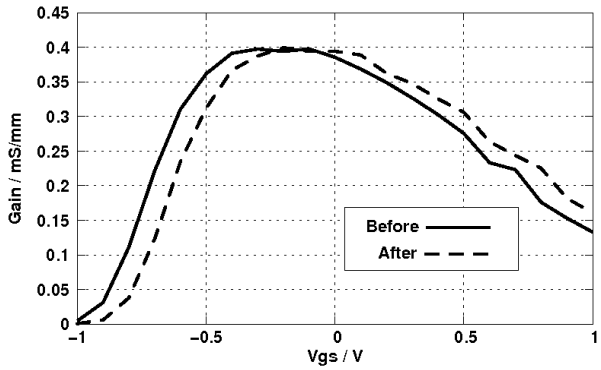

Figure 10: Gm curve before and after stress test of Epi source Q2

This shift is much lower on the standard Epi and also on the Epi from supplier Q2.

CONCLUSIONS

An on wafer test bench is presented to stress transistors under RF conditions and high temperature. The test bench uses mechanical tuners at the output of the Device Under Test to adjust the load impedance within a wide range of $|\Gamma|<0.8$. Therefore, very different types of transistors can be stressed with reasonable load impedances. Furthermore, the degradation dependent on the load impedance can be investigated which results in important information to the designer.

Due to the fast response time this set up is very useful during the development of new technologies to see reliability problems under RF conditions in an early stage of the development. Also the impact of modifications for existing technologies can be treated fast.

ACKNOWLEDGEMENTS

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REFERENCES

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ACRONYMS

WLR: Wafer Level Reliability
pHEMT: Pseudomorphic High Electron Mobility Transistor
DUT: Device Under Test
HTOL: High Temperature Operating Life-Test
RF: Radio Frequency
Lg: Gate Length
Vbds: Transistor Break Down
Vds: Drain Source Voltage
Vgs: Gate Source Voltage
Ids: Drain Source Current