Processing Methods for Low Ohmic Contact Resistance in AlN/GaN MOSHEMTs

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Abstract

In this work, we demonstrate various ohmic contact formation processes using an AlN/GaN (MOS)HEMT structure with an aluminum oxide gate dielectric formed by ALD. The MOSHEMT structure is advantageous because the thin oxide layer protects the ultra-thin (~3 nm) AlN barrier against exposure to the processing chemicals. Contact resistance values as low as 0.457 Ω·mm are reported on TLM structures. The corresponding devices exhibited excellent electronic transport properties with room temperature mobility $\mu > 1000$ cm^2/V·s and sheet carrier concentration $n_S > 3.25 \times 10^{13}$ cm^{-2}. These are the lowest contact resistance values obtained for AlN/GaN HEMTs in the high mobility range (> 1000 cm^2/V·s).

INTRODUCTION

Al(Ga)N/GaN HEMTs have proven to be a breakthrough technology for high-speed, high-power electronics [1]. The conventional AlGaN/GaN layer structure offers several advantageous metrics such as high RT mobility, high saturation velocity, and ultra-thin barrier scaling to obtain exceptional cutoff frequencies. However, the 2DEG charge density is limited by the polarization-induced electric field which presents a challenge to increase the drain-source current for high-power applications.

By eliminating gallium in the barrier layer, all-binary AlN/GaN HEMTs are theoretically superior to any other III-V nitride-based heterostructure [2]. The reason is attributed to the maximum possible spontaneous and piezoelectric difference between the epitaxial AlN barrier and underlying GaN [3]. As a result, several record device performance parameters have been reported: sheet carrier densities $> 4 \times 10^{13}$ cm^{-2} [4] (theoretical limit: ~6 x 10^{13} cm^{-2}), sheet resistance values as low as ~100 Ω/□ [4], output current density > 2.3 A/mm [5], and cutoff frequency over 105 GHz [6],[7].

The AlN barrier can be scaled to ultra-thin barriers due to the large polarization difference of AlN/GaN; thus, reducing short channel effects and increasing frequency performance [8]. Studies have shown strain relaxation in AlN/GaN HEMTS occurs for barrier thicknesses > 60 Å, and device results have been reported for AlN barriers as thin as 23 Å [9]. According to [8], this translates to realistically surpassing W-band cutoff frequencies without adverse short-channel effects.

Despite many AlN barrier advantages, there are some drawbacks worth noting. Among them, ultra-thin AlN barriers are very susceptible to gate leakage and channel depletion due to surface effects. As a solution, a MOSHEMT device structure was implemented with an aluminum oxide dielectric layer deposited above the AlN barrier. High-k dielectrics such as aluminum oxide are preferred to minimize both the resultant shift in threshold voltage, V_T, and decrease in transconductance, g_m [10]. A thin GaN cap layer (~10 Å) was also grown above the AlN barrier to reduce both surface oxidation and the ohmic Schottky barrier height [11]. A representative AlN/GaN MOSHEMT device cross section is shown in Fig. 1.
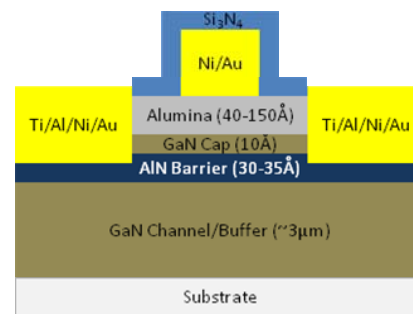

Fig. 1: Representative AlN MOSHEMT device structure cross-section.

Unfortunately, the highly anticipated theoretical operating limits are often affected by poor ohmic contact resistance. The primary contribution remains under investigation; however, various semiconductor processing chemicals such as developers (i.e.: AZ400K) are known to degrade and slowly etch AlN [12]. Using the MOSHEMT device structure is advantageous as the AlN remains unexposed during processing with the exception of ohmic contact formation. This paper investigates processing techniques for removing the alumina dielectric prior to ohmic metallization to form low ohmic contact resistance.

TABLE 1
SUMMARY OF PROCESSED SAMPLES

Sample ID	Alumina thick. (Å)	GaN cap / AlN barrier thick. (Å)	Pre-metal dip (sec)	Substrate	Alumina Etch Type	Time (sec)	Etch Details
A	150	10/27	30	Sapphire	Dry Etch - ICP	25	BCl_3/Cl_2
B	150	10/27	--	Sapphire	Wet Etch	30	1:1 $BOE:H_2O$
C	150	10/27	--	Sapphire	Dry Etch - ICP	10	BCl_3/Cl_2
D	40	10/35	--	6H-SiC	Dry Etch - RIE	120	CF_4/CHF_3

REVIEW OF AlN HEMT OHMIC CONTACT PROCESSING

Low ohmic contact research for AlN/GaN HEMTs has uncovered interesting developments. Recently, the Univ. of Notre Dame group observed that obtaining low ohmic contact resistance is dependent on the quality of the AlN thin-film (measured in terms of carrier mobility). They obtained ultra-low contact resistance of ~0.3 Ω·mm on AlN with ~300 $cm^2/V·s$ mobility and > 1 Ω·mm on AlN with > 1000 $cm^2/V·s$ mobility [6]. Wang, *et. al.,* further discovered diffusion stems developed in the AlN layer forming large TiN "spikes" in the GaN buffer layer. The Ti/AlN reaction was restricted by a nucleation barrier, and electrons were capable of tunneling through the AlN barrier. Ohmic contact resistance as low as 0.455 Ω·mm was obtained using a Ti/Al/Mo/Au ohmic metal stack on a 3-nm AlN barrier, but the carrier mobility was not reported [11]. In this paper, we report 0.457 Ω·mm ohmic contact resistance on TLM structures with locally tested carrier mobility > 1000 $cm^2/V·s$.

FABRICATION AND EXPERIMENT

AlN/GaN HEMT structures were grown on c-plane sapphire and semi-insulating 6H-SiC in a MBE system equipped with an RF nitrogen plasma source (SVTA-RF45). The growth process started with surface preparation at high temperatures by either removing the surface oxides, in the case of SiC, or nitridation using RF plasma source, in the case of sapphire, followed by the growth of a thin AlN nucleation layer. Next, 3 μm of low-defect GaN buffer was grown. A relatively low dislocation density (~ 1×10^9 cm^{-2}) in these films was confirmed previously by both etch pit density measurements, using AFM, and by TEM. Finally, the AlN/GaN active layer was formed by growing a thin (3-4 nm) AlN layer at about 700 °C. The epitaxial structure was finished by depositing ~1 nm of protective undoped GaN cap-layer. The AlN/GaN surface was further protected by growing a 4-15 nm Al_2O_3 layer formed by ALD in a separate vacuum chamber.

AlN/GaN MOSHEMT devices were fabricated using conventional processing techniques. Mesa isolation was performed using a standard BCl_3 recipe in a PlasmaTherm 770 ICP system. A Ti/Al/Ni/Au ohmic metal stack was evaporated and annealed in a nitrogen environment. Two-finger Ni/Au gates were deposited with a gate length variation from 1 μm (optical) to 150 nm using electron-beam lithography. The devices were passivated with 1000 Å PECVD SiN deposited at 300°C.

Sample preparation varied prior to ohmic metal deposition. For each sample, ohmic contact lithography was performed using an SF11/1805 photoresist stack followed by a two-minute oxygen plasma ash to remove residual photoresist. The alumina dielectric was etched prior to depositing ohmic metal. A summary of the etch techniques is shown in Table 1. Dry and wet etch rates were calibrated on samples with thick ALD alumina grown on silicon and analyzed using a Zygo Interferometer. One sample was also dipped in a pre-metallization solution of 1:1 $HCl:H_2O$ before depositing ohmic metal.

RESULTS AND DISCUSSION

Ohmic contact resistance measurements were obtained from TLM device structures using a Keithley 450 parameter analyzer. Test results, shown in Fig. 2, clearly indicate that Sample C processing methods produced the best results with an average of 0.59 Ω·mm (14% std. deviation). Several reticles measured below 0.50 Ω·mm with the lowest R_C measuring 0.457 (with > 99.9% fit accuracy) on Sample C. Sample D yielded very high resistance indicating either the alumina was not etched or the RIE etch damaged the 2DEG.
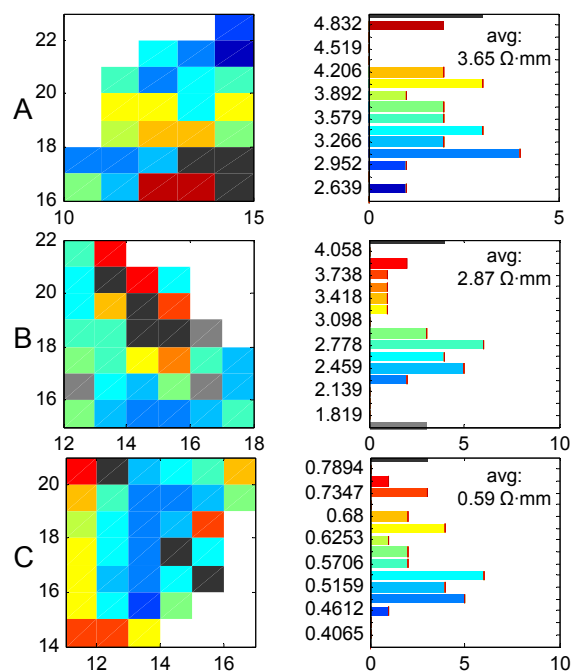

Fig. 2: Wafer map view of ohmic contact resistance measurements for each quarter sample.

Sample C was further characterized due to its excellent ohmic contact resistance. On-wafer RT Hall measurements were performed for select reticles to investigate the relationship between low ohmic contacts and AlN thin-film carrier mobility. Measurements were conducted on passivated Van der Pauw PCM structures located near the TLM test structure in each reticle. A TEM cross section was also obtained to verify the layer thickness shown in Fig. 3.
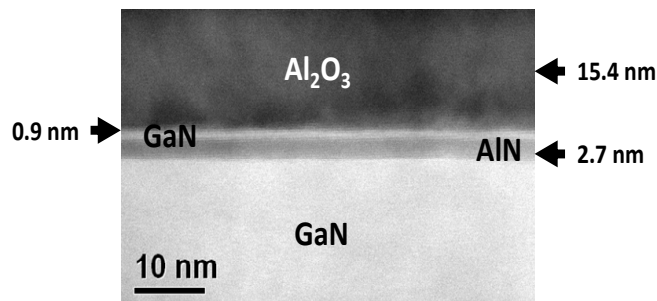

Fig. 3: TEM image of layer cross-section for Sample C.

Hall measurements were used to verify that low ohmic contacts were achieved with carrier mobility > 1000 cm²/V·s. Very high sheet carrier densities were also recorded exceeding 3.25×10^{13} cm⁻² along with excellent sheet resistance values of ~161 Ω/□. The dependence of carrier mobility and contact resistance was not apparent during this experiment. The results of select reticles from Sample C are plotted in Fig. 4.
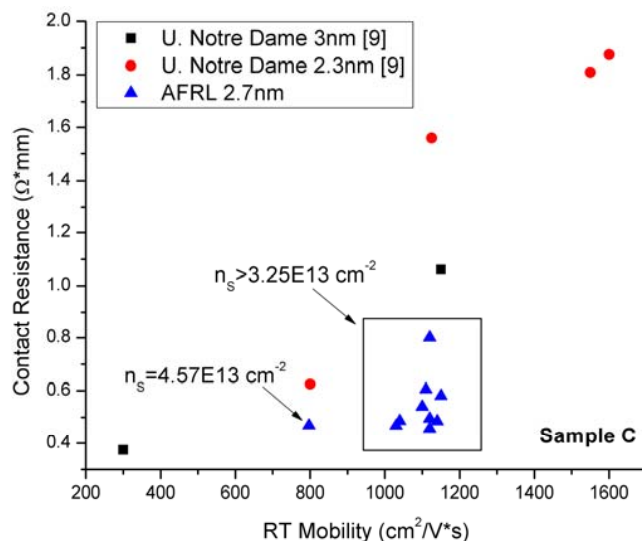

Fig. 4: Contact resistance as a function of room temperature mobility for select reticles of Sample C.

The pre-metallization etch profile was studied with limited success. A TEM image, shown in Fig. 5, confirmed the alumina dielectric, GaN cap, and nearly the entire AlN layer were affected by either the ICP etch or alloy in Sample C (reticle with $R_C = 0.457$ Ω·mm). TEM chemical analysis did

not detect any aluminum at the contact interface despite the excellent contact resistance of the sample. We postulate that the AlN layer was etched so thin it was not detectable, and the surface was rough to allow intermittent contact of the annealed metal to the 2DEG channel.
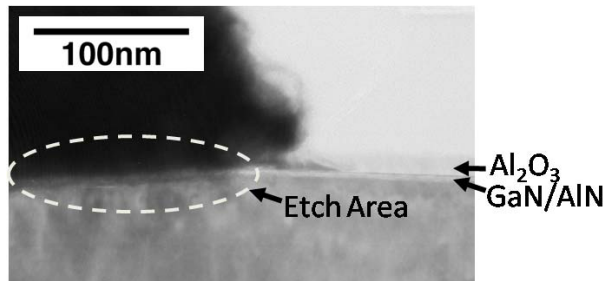

Fig. 5: TEM image of the ohmic metal and semiconductor interface for Sample C indicating the alumina, GaN cap and nearly all the AlN was etched prior to depositing ohmic metal.

Two-finger MOSHEMT transistor structures were tested on Sample C. DC I-V characterization, shown in Fig. 6, revealed ~1.1 A/mm drain-source current and an extrinsic transconductance of 246 mS/mm for e-beam T-gates with L_G = 250 nm. For L_G = 150nm, the average cutoff frequency, f_t, and maximum frequency, f_{max}, were 25 GHz and 22 GHz, respectively. The gate was biased up to +4 V; however, beyond +2 V we noticed thermal effects. It is worth noting that despite excellent device parameters the open channel current remained below 1 A/mm, and the buffer isolation current was unusually high. More research is necessary to determine the underlying issue that prevents the device from reaching theoretical limits. If these material parameters can be repeated, $\mu > 1100$ cm²/V·s, $n_S > 3.25 \times 10^{13}$cm⁻², $R_{SH} <$ 165 Ω/□, and $R_C < 0.5$ Ω·mm, potentially record-breaking device performance can be demonstrated .
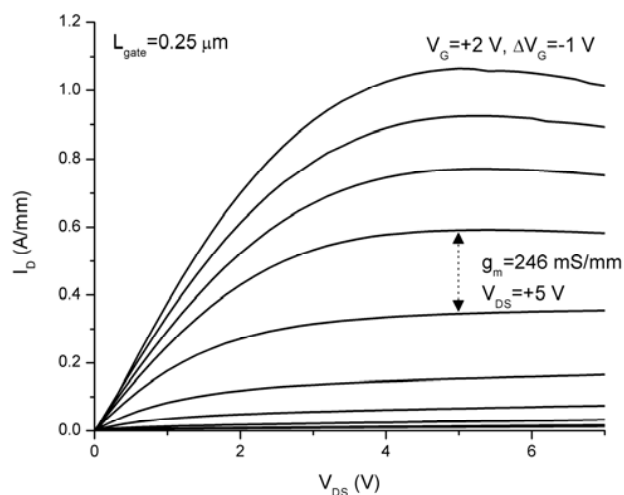

Fig. 6: DC I-V curves for Sample C showing drain-source current of ~1.1 A/mm and extrinsic transconductance of 246 mS/mm.

CONCLUSIONS

Various ohmic contact processes were presented using an AlN MOSHEMT device layer structure. Low ohmic contact resistance was demonstrated using a timed low-power ICP etch of the ALD alumina layer prior to ohmic metallization. Devices showed low ohmic contact resistance of 0.457 $\Omega \cdot$mm with excellent mobility, sheet charge density, and sheet resistance. Such devices are capable of high performance for future W-band and millimeter-wave applications.

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ACRONYMS

2DEG: Two-Dimension Electron Gas
AFM: Atomic Force Microscopy
ALD: Atomic Layer Deposition
BOE: Buffered Oxide Etch
HEMT: High Electron Mobility Transistor
ICP: Inductively Coupled Plasma
MBE: Molecular Beam Epitaxy
MOSHEMT: Metal-Oxide-Semiconductor HEMT
PCM: Process Control Measurement
PECVD: Plasma Enhanced Chemical Vapor Deposition
RIE: Reactive Ion Etch
RT: Room-temperature
TEM: Transmission Electron Microscope
TLM: Transmission Line Measurement