SiC Backside Via-hole Process For GaN HEMT MMICs
Using High Etch Rate ICP Etching

Naoya Okamoto, Toshihiro Ohki, Satoshi Masuda, Masahito Kanamura, Yusuke Inoue, Kozo Makiyama,
Kenji Imanishi, Hisao Shigematsu, Toshihide Kikkawa, Kazukiyo Joshin, and Naoki Hara

Fujitsu Limited and Fujitsu Laboratories Ltd.

10-1 Morinosato-Wakamiya, Atsugi 243-0197, Japan

E-mail: naoya_okamoto@jp.fujitsu.com, Phone: +81-46-250-8242

Abstract

We have demonstrated a SiC backside via-hole process for GaN HEMT MMICs using ICP etching at a high rate of about 2 μm/min, higher than any previously reported rate. We discuss pillars, microtrenches, RIE lag, loading effects and etch uniformity in high-rate ICP etching, which are significant issues related to the yield of via-hole fabrication. Finally, we describe the successful 3-inch backside via-hole process for GaN HEMT MMICs.

INTRODUCTION

SiC backside via-holes are a key technology in realizing GaN HEMT MMICs for millimeter-wave high-power amplifiers [1, 2]. However, SiC is a very difficult material to etch due to the high Si-C bond energy. Thus, the SiC etch rate for dry etching has been reported to be about 1 μm/min or less [3, 4], which is insufficient for fabricating via-holes, unlike conventional GaAs dry etching [5]. Furthermore, micromasking forms pillars that create an obstacle to metallization in the via-holes, and trenching leads to punch-through of the front-side metal. These problems cause degradation in the yield of via-hole fabrication. Therefore, it is doubtful whether dry etching is suitable for mass production of GaN HEMT MMICs with via-holes in contrast to extreme high-rate laser drilling for one of the via-holes [6]. However, we believe that solving these problems would enable effective ICP etching for simultaneously fabricating via-holes at a high density in a large wafer. In addition, we could use the existing processing for GaAs devices, which would reduce the investment in process equipment.

In this study, we demonstrate a SiC backside via-hole process for GaN HEMT MMICs using ICP etching at a high rate of about 2 μm/min, higher than any previously reported rate. Furthermore, pillars, microtrenches, RIE lag, loading effect and etch uniformity are discussed as significant issues related to the yield of via-hole fabrication. Finally, we demonstrate the 3-inch SiC wafer backside via-hole process.

EXPERIMENTAL

We used 4H-SiC (0001) substrates. An electroplated Ni metal mask with diameter openings of 50-150 μm was fabricated on SiC substrates. Etch experiments were performed using an ICP system in which RF (13.56 MHz) power was supplied to the ICP coil and platen. Etching in mixtures of SF_6 and O_2 was carried out. Samples were bonded onto the carrier by high-temperature-resistant thermoplastic adhesion. The backside of the carrier was cooled with He. Etched samples were evaluated using SEM and CLSM.

RESULTS AND DISCUSSION

A. HIGH-RATE ICP ETCHING AND ITS ISSUES

Figure 1 shows SEM images of a typical 160-μm-deep SiC via-hole 100 μm in diameter fabricated for 80 min at an etch rate of 2 μm/min. Then, the ICP coil and platen power were set to 2 and 0.2 kW, respectively. The SF_6 and O_2 flow rates were fixed at 200 and 10 sccm, respectively. The operating pressure was 10 Pa. The anisotropic etch profile has a vertical sidewall without an undercut for the Ni metal mask. In addition, the microtrenches observed at the etched bottom of the via-holes were very small. However, we found large pillars in another via-hole of the same sample, as shown in Fig. 2.

To understand the mechanism of pillar formation, we examined in detail the etched bottom surface of a via-hole by using SEM. Various features could be observed at the etched bottom surface of via-holes, as shown in Fig. 3. A cap-shaped structure (a) and needle-shaped structure (b) can be seen in the center of the dip structure on the same etched bottom surface of the via-holes. These features on the right suggest the occurrence of a pillar formation process. According to our study [7], this cap-shaped structure is

referred to as being the origin of micropipes involved with SiC. Since the origin of micropipes has a slower etch rate due to stoichiometry that differs from SiC, it acts as a micromask. In addition, the origin of micropipes is passivated by non-volatile and difficult-to-etch products of NiSiF, which are generated by a chemical combination of etched Ni from the metal mask and SiF_X species formed during etching, as shown in Fig. 4. Thus, the cap-shaped structure would grow into needles and pillars. This problem will be solved in the future by using perfectly micropipe-free SiC substrates. However, as micropipes are practically involved with SiC, it is indispensable to eliminate these pillars that will hinder metallization in the via-holes. Therefore, we optimized the etching conditions to eliminate them. Consequently, by decreasing the operating pressure at an O_2 flow rate of 10 sccm to enhance Ni desorption from the via-holes, we eliminated the pillars in SiC via-holes, as shown in Fig. 5(a). In addition, a high etch rate of 2 µm/min and high etch selectivity of over 100 for Ni were obtained at a pressure of 5 Pa. However, this resulted in a maximum trenching amount, as shown in Fig. 5(b). The trenching amount was defined as the ratio of microtrench depth to via-hole depth. Additional examination successfully minimized the trenching by increasing the O_2 flow rate up to 20 sccm while maintaining the etch rate of 2 µm/min and the etch selectivity over 100.
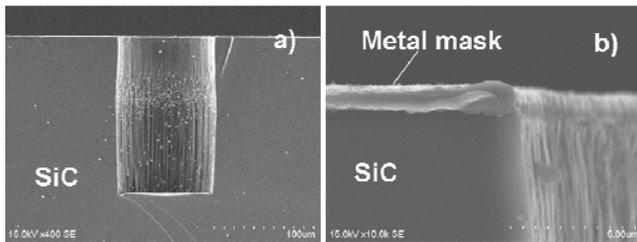

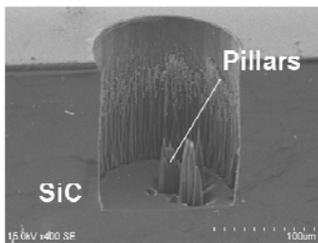Fig.1. SEM images of typical 160-µm-deep SiC via-hole 100 µm in diameter.

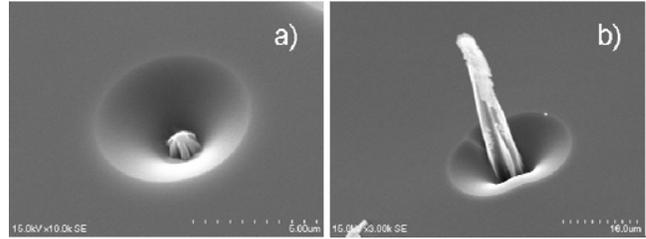Fig.2. Pillars formed in a via-hole.

Fig.3. SEM images of etched bottom surface in via-hole.
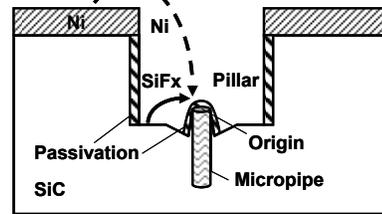

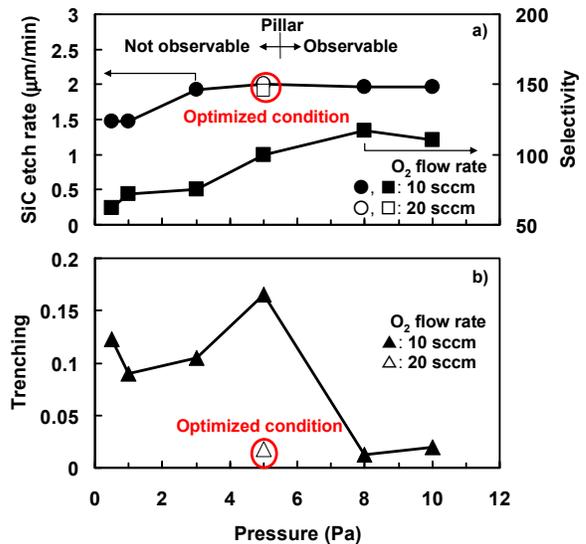Fig.4. Pillar formation associated with micropipe in SiC.

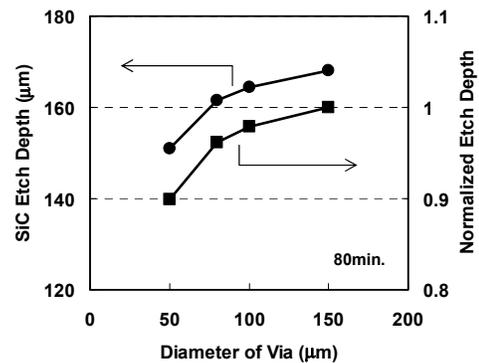Fig.5. Pressure dependence of etch rate, selectivity and trenching amount.

Fig.6. Via size dependence of SiC etch depth.

Next, since the stability of the etch rate is also directly related to the yield of via-hole fabrication, we examined the RIE lag and loading effects as significant issues leading to uneven etch rate. Figure 6 indicates the RIE lag at an etch time of 80 min. The etch depth decreased to 90 % by reducing the diameter of via-holes from 150 to 50 μm. Therefore, it is desirable to unify the size of via-holes for MMIC design. On the other hand, no loading effect was observed as far as we investigated when the area of via-holes was 12.3% or less. Additionally, we found that there was a large difference in etch rate between semi-insulating and n-doped SiC in high-rate ICP etching, as described elsewhere [8]. However, these issues are controllable through precise prior examination.

Finally, we evaluated the uniformity in etch depth across a 3-inch SiC wafer by using CLSM, as shown in Fig. 7. The etch time was 80 min. Then, the average etch depth was 160 μm, corresponding to the etch rate of 2 μm/min. Excellent uniformity in etch depth, within ±4.1%, was obtained.

As described above, we succeeded in solving several severe problems with regard to high-rate ICP etching of SiC. These results indicate that ICP etching is suitable for mass producing GaN HEMT MMICs with via-holes.
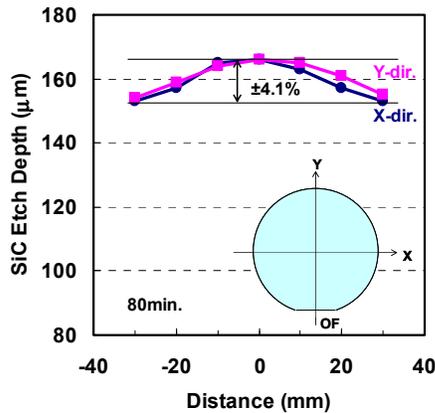

Fig.7. Variation across a 3-inch SiC wafer in etch depth.

B. 3-INCH VIA-HOLE PROCESS

The 3-inch SiC backside via-hole process was carried out according to the flow chart illustrated in Fig. 8. First, the front-side etch stopper consists of a vacuum-evaporated 100-nm Ni/350-nm Au layer and electroplated 3-μm Au layer. After the 3-inch wafer was protected with high-temperature-resistant polymer, and then bonded onto a 4-inch transparent sapphire carrier by thermoplastic adhesion, it was thinned to a thickness of 50 μm. In order to determine the etch time, we precisely evaluated the thickness by using CLSM without destroying it before etching. We calibrated beforehand the thickness of SiC evaluated by

CLSM to the thickness measured by SEM. Then, the SiC refractive index is referred to as being 2.75 at a wavelength of 408 nm. Consequently, the thickness uniformity across the 3-inch wafer was within ±3%.

After that, a Ta/Cu seed metal layer was deposited by sputtering on the backside wafer together with the carrier. After a positive photoresist was patterned using a double-side view aligner, a 2.4-μm-thick Ni metal mask was electroplated. The seed metal layer was etched by Ar ion milling. Figure 9 shows the front- and backside views of the wafer bonded onto the carrier after fabricating the Ni metal mask. In this case, there were about 5,000 via-holes 100 μm in diameter in the 3-inch wafer.

In order to etch over by 10 μm, we determined that the etch time was 30 min at an average etch rate of 2 μm/min. Figure 10 shows the distribution of visible surface of the etch stopper in the 3-inch wafer. Consequently, as shown in Fig. 10(a), the Ni surface appeared in the area from Φ46 mm to the wafer edge. However, in the area from Φ36 to 46 mm, part of the Ni was etched and Au was seen in the center of the etch stopper. Furthermore, in the area within Φ36 mm, Au appeared completely. Taking into account etch uniformity, the estimated SiC etch depth was 62.4 and 57.6 μm in the center and at the edge of the 3-inch wafer, respectively. When the etch selectivity is 100, 10-μm-thick SiC corresponds to 100-nm-thick Ni. Therefore, it is reasonable that Ni would be completely removed from the center of the wafer but still remain at the wafer edge. To stop the etching on Ni in the entire 3-inch area, it would be necessary to further increase the thickness of Ni or improve the etch uniformity.
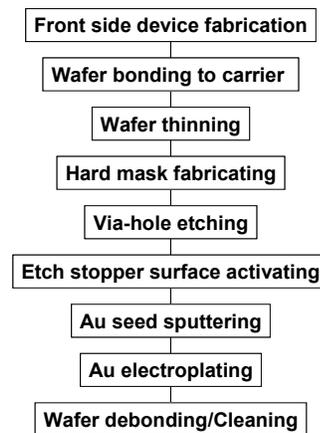

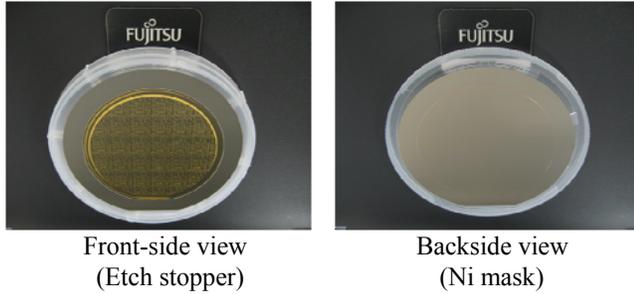Fig.8. Flow chart of 3-inch SiC backside via-hole process.

Front-side view   Backside view
(Etch stopper)   (Ni mask)
Fig.9. 50-µm-thick 3-inch SiC wafer bonded on carrier.

Since the surface of the etch stopper is exposed to SF_6/O_2 plasma during etching, it may become electrically inactive. Therefore, it is necessary to remove any contamination from the etch stopper. However, in the wet-process, acid may penetrate the front-side device, resulting in corrosion. Thus, in order to clean the exposed surface of the etch stopper, we selected Ar ion milling as a dry-process. As shown in Fig.10 (b), the visible surface of the etch stopper in the entire area became Au after Ar ion milling.

After that, a Ti/Au seed metal layer was deposited on the wafer by sputtering, and then a 12-µm-thick Au layer was electroplated. The electroplated Au seems to be smoothly connected to the etch stopper in Fig. 11.

Finally, the processed wafer was successfully demounted from the carrier without cracking, after that the thermoplastic adhesive and protection polymer were removed with the respective solvents.

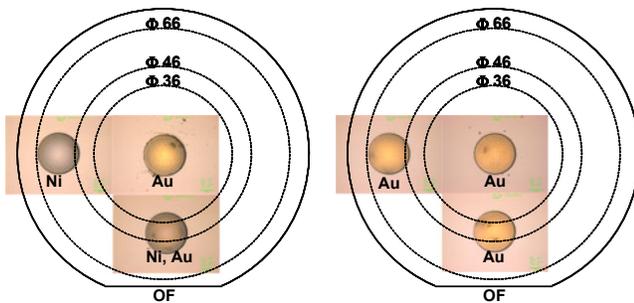a) After ICP etching   b) After Ar ion milling
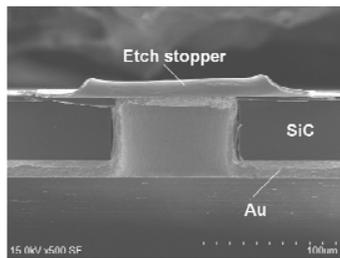Fig.10. Distribution of visible surface of etch stopper in 3-inch wafer.

Fig.11. SEM image of via-hole after Au electroplating.

C. VIA INDUCTANCE

We measured the inductance of a 100-µm-deep SiC via-hole 70 µm in diameter, which was fabricated by using the same 3-inch backside via-hole process. Then, a "*surface-charge-controlled*" GaN HEMT structure [9] was also included and etched by employing SF_6/O_2 under the same conditions because it was very thin, although etch selectivity was 30 to 50. As a result, the inductance of this via-hole was 20 pH. This indicates that our developed via-hole process is highly feasible for fabricating GaN HEMT MMICs. The good performance of GaN HEMT MMICs fabricated using this via-hole process will be demonstrated elsewhere [2].

CONCLUSIONS

We demonstrated a SiC backside via-hole process for GaN HEMT MMICs using ICP etching at a high rate of about 2 µm/min, higher than any previously reported rate. Additionally, significant issues such as pillars, microtrenches, RIE lag, loading effect and etch uniformity in high-rate ICP etching were discussed. Finally, we described the successful 3-inch backside via-hole process for GaN HEMT MMICs.

REFERENCES

[1] Y. Inoue *et al.*, *A CW 7-12 GHz GaN Hybrid Power Amplifier IC with high PAE using the Load-Impedance Change Compensation Technique*, IEEE CSICS Technical Digest, October 2008.

[2] S. Masuda *et al.*, *W-band GaN MMIC Amplifiers with Grounded Coplanar Waveguide*, IEEE RF-IC Technical paper, June 2009 (submitted).

[3] P. Chabert, *Deep etching of silicon carbide for micromachining applications: Etch rates and etch mechanisms*, J. Vac. Sci. Technol. B19 (2001) 1339.

[4] L. F. Voss *et al.*, *SiC via fabrication for wide-band-gap high electron mobility transistor/microwave monolithic integrated circuit devices*, J. Vac. Sci. Technol. B 26 (2008) 487.

[5] For example, R. Westerman *et al.*, *Eliminating Pillars During GaAs Via Etch Formation*, 2003 GaAs MANTECH Technical Digest, May 2003.

[6] T. Anderson *et al.*, *Laser ablation of via holes in GaN and AlGaN/GaN high electron mobility transistor structures*, J. Vac. Sci. Technol. B24 (2006) 2246.

[7] N. Okamoto, *Elimination of pillar associated with micropipe of SiC in high-rate inductively coupled plasma etching*, J. Vac. Sci. Technol. A27. Mar/Apr 2009 (to be published).

[8] N. Okamoto, *Differential etching behavior between semi-insulating and n-doped 4H-SiC in high-density SF_6/O_2 inductively coupled plasma*, J. Vac. Sci. Technol. A. (submitted).

[9] T. Kikkawa *et al.*, *Surface-charge-controlled AlGaN/GaN-power HFET without current collapse and Gm dispersion*, IEEE IEDM Technical Digest, pp. 585-588, December 2001.

ACRONYMS

HEMT: High Electron Mobility Transistor
MMIC: Monolithic Millimeter-wave Integrated Circuit
ICP: Inductively Coupled Plasma
RIE: Reactive Ion Etching
RF: Radio Frequency
SEM: Scanning Electron Microscope
CLSM: Confocal Laser Scanning Microscope