High-Volume 0.25 µm AlGaAs/InGaAs E/D pHEMT Process Utilizing Optical Lithography

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Abstract

TriQuint has developed a 150 mm high-volume 0.25 µm enhancement / depletion (E/D)-mode pseudomorphic high-electron mobility (pHEMT) AlGaAs / InGaAs based transistor process. Released as TQP25, the 0.25 µm gate length target is possible by utilizing a sidewall spacer process and is a hybrid of TQPED (0.5 µm) and the TQP13 (0.13 µm) pHEMT processes from TriQuint. Typical Depletion-FET (DFET) parameters include a 50 GHz unity current gain cut-off frequency (Ft), -900 mV pinchoff voltage, 550 mA/mm Imax (Vgs = 0.9V), 1.0 Ω-mm on resistance, and a 12 V minimum breakdown voltage. Additionally, the TQP25 process presented here includes a 0.35 µm Enhancement-FET (EFET) not typical at this technology node. Nominal EFET parameters are a 45 GHz Ft, a 300 mV threshold voltage, 1.3 Ω-mm on-resistance, and a 12 V minimum breakdown voltage. Passive components include two thin film resistor options (50 Ω/square and 1KΩ/square), a 0.62 fF/µm^2 MIM capacitor and 1 local layer of evaporated interconnect and 1 global planarized plated metal layer. TQP25 allows designers to create circuits ranging in diverse applications from the cellular band to K_u-band.

INTRODUCTION

This paper introduces the most recent addition to TriQuint's growing family of mature and high-yielding sidewall spacer technologies; a process that features both a double recessed 0.25 µm DFET and a 0.35 µm EFET. This combination, called TQP25, allows for functionality typically seen at the 0.5 µm node. Due to the reduced gate length, higher frequency DFET and EFET designs and E/D logic blocks are realized. Additionally, the aggressive TQP25 layout design rules, the low off-capacitance, (250 pF/mm) and on resistance of 1.0 Ω-mm allow very high performance switches, LNAs, and power amplifiers. This process allows a unique design flexibility spanning the range between handset cellular bands through the X-band application space.

TQP25 is manufactured on 150 mm substrates using etch, photo, physical and chemical vapor deposition (PVD/CVD) and metal deposition tools that are already in use in the production line at TriQuint. To achieve the 0.25 um node and lower, TriQuint utilizes a standard I-Line stepper technology and avoids the higher cost and lower yield associated with the typical electron-beam or deep-UV stepper gate formation found on other sub 0.5 µm processes [1-3].

PROCESS ARCHITECTURE

TQP25 development was based on a hybrid between TriQuint's double recessed 0.5 µm E/D process (TQPED) [4] and the 0.13 µm DFET process (TQP13) [5].

The process begins with AlGaAs/InGaAs Schottky and channel layers, double delta doped to achieve the desired FET parameters. On top of the Schottky, a narrow recess is formed in a GaAs cap layer. Above the GaAs cap layer, a thin AlGaAs layer is added that performs as the wide recess etch stop. Continuing above the etch stop is a N- / N+ doped upper cap optimized for low ohmic contact resistance.

The processing continues by etching the photo alignment marks and the active device wide recess. The recessing is performed via a low damage dry etch process. After the thin AlGaAs etch stop is removed, a blanket plasma oxide (POX) is deposited and the wafers then go through the photo-defined isolation implant process.

The wafers then undergo the gate photo process, where a target, well above the minimum resolution of the I-Line steppers, is selected to serve as an oxide etch window that sets the stage for the narrow recess process. This gate step is the start of the spacer process, where a very wide and manufacturable gate critical dimension (CD), ultimately translates down to a 0.25um target, without the need for an expensive electron beam process or a deep-UV stepper to achieve gate lengths 0.25um and below.

At this point, the POX is etched through the gate photo resist, the resist is stripped, and then the GaAs cap is dry etched in the same tools as the previous wide recess step. The AlGaAs Schottky layer serves as the narrow recess etch stop. The narrow recess is formed simultaneously for both the D and the EFETs at this step.

Gates formed by oxide spacer deposition and etch back methods has been covered in detail in reference [5] and is widely used in the Silicon CMOS industry, so the details will not be provided here. Nevertheless, after the narrow recess, a blanket POX is deposited and etched back using the

same dry etch toolset, however in a chamber tailored for oxide etching. The spacers take the gate from the narrow recess CD down to the final gate length target of 0.25 µm.

Next, a blanket refractory metal film is deposited, followed by an evaporated gate reinforcement layer (GMET). The GMET acts as a hard mask for the refractory gate etch back. This is followed up by formation of the non-self aligned Au/Ge/Ni/Au ohmic contacts via a standard photo, deposition, liftoff and anneal process. Figure 1 below shows a cartoon cross-section of a DFET at this point in the process, where the wide and narrow recesses, the gate spacer, and the Dgate metallization can all be visualized.

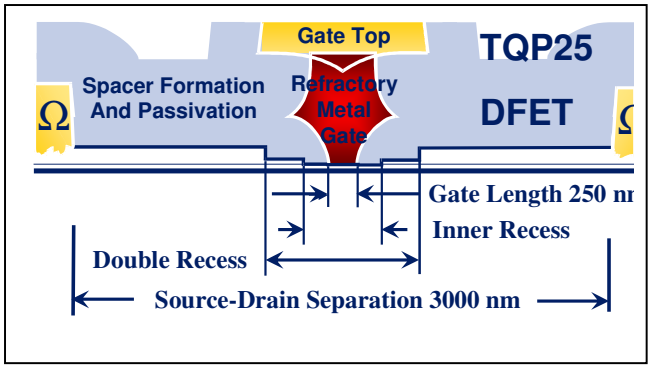

Figure 1: Schematic Cross-Section of a TQP25 DFET.

After an electrical test point, a plasma silicon sitride (PSN) layer encapsulates the DFET gate and ohmic contacts. This is followed by the EFET gate photo process, where an etch window is formed by photo resist and then a spacer in the EFET active areas is formed, again by a modified spacer process. A Pt/Ti/Pt/Au Egate metal stack is sputter deposited and then lifted off. Slight differences between the EFET and DFET spacer etches account for the final 0.35 µm EFET gate length.

Following another PSN deposition, via photo, and etch, a thin film resistor layer process sequence follows. The two thin film resistor options offered on TQP25 are either a 50 Ω/square film or a 1KΩ/square film. Following the resistor module, the ohmic contacts and Egates are connected through a subsequent "Bell Metal" (BLMET) deposition. The BLMET layer is an evaporated Ti/Pt/Au stack 0.62 µm thick with a nominal sheet resistance of 50 mΩ/square. The BLMET layer also forms the bottom plate of the MIM capacitor. The BLMET layer is then covered in a precision MIM dielectric PSN. On top of the nitride layer, a capacitor top (CTOP) layer 0.42 µm thick is evaporated, forming the top plate of the 0.62 fF/um² MIM capacitor.

All of the previous interconnect layers described have been used for local routing. Typically, other processes at the 0.25um node use airbridge interconnects to form a global interconnect layer. In contrast, TQP25 creates a global interconnect on top of a spun-on benzocyclobutene (BCB) planarization layer. Following a second via photo and etch step, a 4 µm thick metal 2 layer is electroplated, finalizing the connections to the active and passive areas of the die. Planarizing the die in this manner, allows for a higher density interconnect and increased flexibility for the circuit designer by allowing bondpads to cover areas of the circuit under the BCB; thereby saving valuable die area, which is not possible in standard airbridge processing. The processing is completed by a final passivation coating and etch of the contact openings, followed by a final DC and RF test sequence.

A designer using TQP25 has a full range of standard high volume backside options including the 4 mil thin and substrate via (SVIA) module or the TriQuint CuFlip™ copper bump process at TriQuint.

DEVICE PERFORMANCE

Table 1 below lists the key specs for the transistors and passive elements of the TQP25 process.

TABLE I
TQP25 PROCESS SUMMARY

Process Specifications, Vds = 3.0 V		
Parameter	**Typical Value**	**Units**
E/D Lg	0.35 / 0.25	um
D-Vp	-0.9	V
E-Vp	0.3	V
E/D-R_on	1.3 / 1.0	Ω-mm
D-C_off	250	pF/mm
E/D BV	12 / 12	V
D-Imax/Idss	550 / 275	mA/mm
E-Imax	300	mA/mm
D-Gm	450 @ Idss	mS/mm
E-Gm	650 @ 50% Imax	mS/mm
D Ft / Fmax	50 / 125 @ Idss	GHz
E Ft / Fmax	45 / 115 @ 50% Imax	GHz
Process Elements		
Parameter	**Typical Value**	**Units**
Resistors	50 / 230 / 1000	Ω/sq
BLMET (0.62um)	50	mΩ/sq
Met 2 (4um)	6	mΩ/sq
MIM Cap	0.62	fF/um^2

Figures 2 and 3 follow showing standard normalized DC Ids-Vds family curves and Ids and Gm vs. Vgs transfer curves respectively for D-mode transistors.

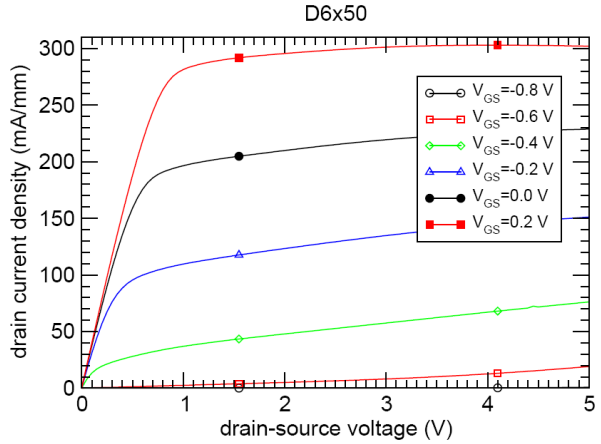

Figure 2: Normalized Ids-Vds family curves for a typical TQP25 DFET.

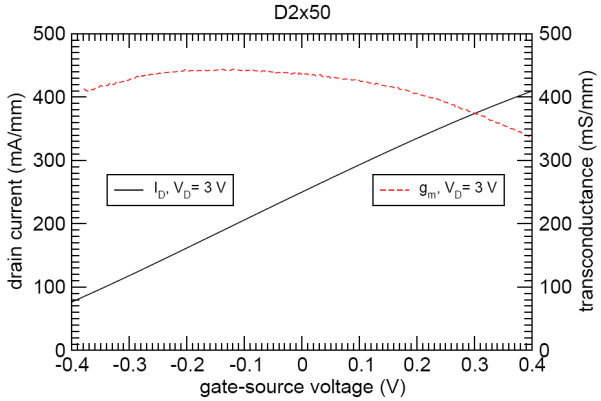

Figure 3: Normalized Ids-Vgs (transfer curves) for a typical TQP25 DFET.

Figures 4 and 5 below show standard normalized DC Ids-Vds family curves and Ids and Gm vs. Vgs transfer curves respectively for E mode transistors.

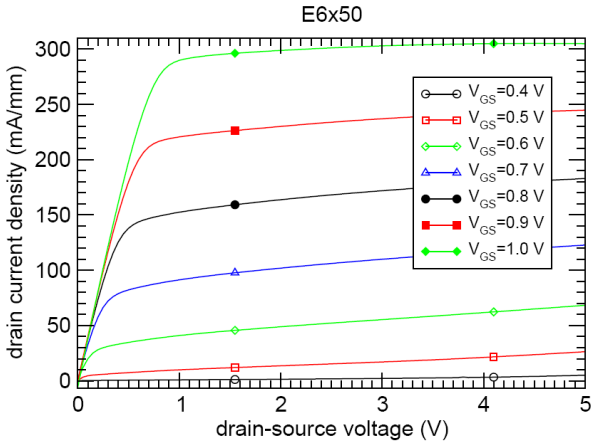

Figure 4: Normalized Ids-Vds family curves for a typical TQP25 EFET.

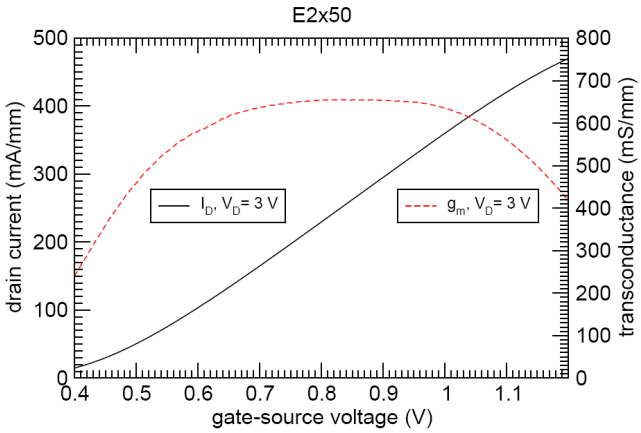

Figure 5: Normalized Ids-Vgs (transfer curves) for a typical TQP25 EFET.

TQP25 DFETs have been successfully evaluated for use in handset switch designs, looking specifically at harmonic and transient response. Figure 6 demonstrates flat harmonic response (no transients) following a RF pulse cycle in a single-pole double throw (SP2T) switch designed using TQP25 under GSM power conditions.

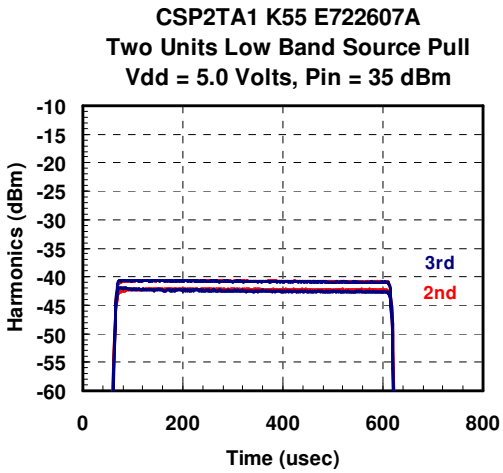

Figure 6: Harmonic response to a GSM burst in a SP2T designed using TQP25 DFETs. No harmonic overshoot is observed.

EFET performance within TQP25 is not simply limited to DC logic functionality. Figure 7 power sweep (load pull) at 1.9 GHz was obtained and the Gain and power-added efficiency (PAE) curves vs. Pin are shown for Vds = 3.0 V and Id = 10 % IDH. IDH is determined by first measuring a gate voltage at which Igs = 1mA/mm (termed VGH). This measured VGH is then applied to the EFET to subsequently determine IDH. A PAE of 70% is demonstrated in Figure 7 when tuned to maximize output power.

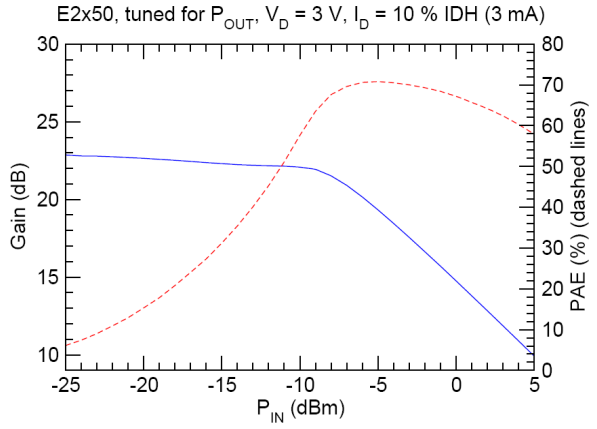

Figure 7: Power sweep curve showing Gain and PAE @1.9GHz for a TQP25 2x50 EFET biased at 3.0 V Vds and 10% IDH.

Figure 8 displays the maximum gain and $|h_{21}|^2$ for 2 different DFET widths and number of fingers. TQP25 DFETs show a typical gain of 11 dB at 30GHz (6 fingers x 50 µm, biased at 45mA, Vds = 4.0V) and a Ft of 50 GHz is determined from the plot, making TQP25 a natural fit for designs up through the X-band (8-12 GHz) and even into the K_u band (12–18 GHz).

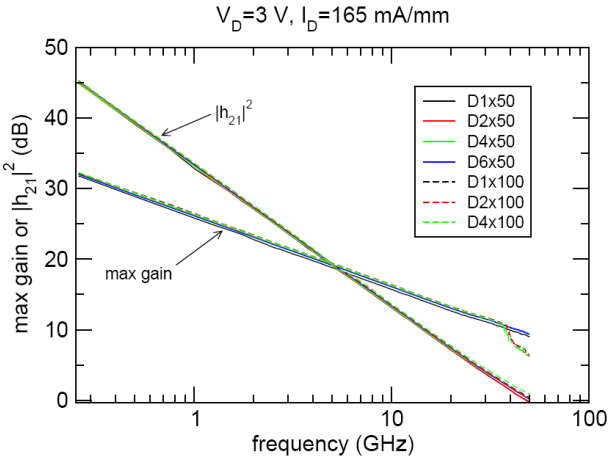

Figure 8: Maximum gain and $|h_{21}|^2$ vs. Frequency for 2 different FET widths with varying number of fingers measured on-wafer at full thickness.

CONCLUSIONS

This paper has introduced a unique new TriQuint process called TQP25. The combination of a 0.25 µm DFET along with a 0.35 µm EFET, using optical stepper technology in a high-volume 150mm wafer production line, allows a cost-advantaged option at the 0.25 µm node not previously available.

A straight-forward development towards a 0.15µm power process in this technology is underway to address the low cost power amplifier markets in the 30- 60 GHz MMW application range.

ACKNOWLEDGEMENTS

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ACRONYMS

pHEMT pseudomorphic high-electron mobility transistor
DFET: Depletion-mode field effect transistor
EFET: Enhancement-mode field effect transistor
GMET: Gate Reinforcement Metal
BLMET: Bell Metal
MIM: Metal Insulator Metal
BCB: Benzocyclobutene
CTOP: Capacitor Top
PAE: Power-added efficiency