SiC Substrate Via Etch Process Optimization

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Abstract

SiC etch rates and etch selectivity to GaN have been studied under a range of RF plasma power conditions. Slightly higher etch rate and higher etch selectivity were obtained at increased coil RF power. Higher etch rate was also obtained at increased platen RF power, but at the sacrifice of decreasing etch selectivity. Substantial pillar formation was observed when coil RF power is below certain limit. Pillar formation during SiC etches due to variation of process conditions was also studied with methods to reduce pillar formation discussed. We observed that by properly modifying pre-etch clean and etch processes, systematic pillar formation can be avoided.

INTRODUCTION

Silicon carbide (SiC) is an attractive wide band gap semiconductor material with high thermal conductivity and high temperature stability, suitable for high power MMIC applications. SiC is also used as a substrate for epitaxial growth of GaN for high power MMIC devices [1]. After transistors are fabricated, electric connection is often made through the backside of the device (through backside via) to further improve device performance.

Thus for the fabrication of SiC based devices, either devices built directly on SiC, or GaN devices using SiC as substrate, high SiC etch rates with high etch selectivity to etch mask materials are required. Ni is often used as the etch hard mask. SiC to Ni etch selectivity around 45:1 has been reported [2]. In several early studies, SiC etch rate $\leq$ 0.6 um/min has been reported [3-9], but there are more recent studies that reported higher etch rate, in the range of 1.5 – 2.7 um/min [2, 9]. For this work our nominal etch rate was 1 um/min.

While previous reports emphasized a desirable high SiC etch rate, there was no mention of process sustainability. In practice, long tool up time is equally important as high etch rate. Often, long tool up time with moderate etch rate is more desirable than short tool up time at a higher etch rate. For example, we observed that once a SiC etch chamber was open to air for wet clean, subsequent process performance deteriorated substantially. The primarily failure was due to micro-masking inside SiC via which resulted gross pillar formation and essentially prevented further SiC etch. Recovery from the wet clean up without modification of the process condition entailed replacement of equipment parts. This replacement is both costly and time consuming, significantly reduces tool availability. This is an example when excellent process results were obtained initially using new equipment hardware, but the result could not be repeated once the hardware is slightly aged and subjected to exposure to air and wet clean. It is critically important to eliminate the strong equipment age and condition dependence on the rate and etch result in order to be able to maintain the process in a mass production environment. In this paper we report the result of pre-etch clean and etch process effect on pillar formation. Pillar formation and etch rate as a function of process RF power are also reported.

EXPERIMENT

A Surface Technology System's (STS) inductively coupled plasma (ICP) tool with optimized ICP source was used for this study. For etch rate and selectivity studies, SiC samples were 6H n-type SiC. GaN samples were GaN grown on SiC; and Ni samples were Ni film evaporated onto Si. A piece of each of these three samples (each about ~1cm x 1cm in size) was mounted onto a Ni-plated Si substrate and was partially covered with Kapton tape to leave an un-etched reference region. Etch was conducted on all three samples at the same time. The mask tape was removed and sample surface was cleaned after etch. Step heights between etched and un-etched regions were measured using a profilometer. Etch was conducted in the range of coil power from 1500 W to 2500 W and platen RF power from 150 W to 300 W.

For pillar formation studies, SiC samples were first ground to remove about 10 um of SiC, then polished to remove another 1 um of SiC. Samples were patterned to form via pattern (~60 um via diameter) with Ni as the hard mask. Sample was also cut into small pieces (~1cm x 1cm) and mounted onto carrier wafers. We used Si, glass, and sapphire (all plated with Ni) as carrier wafers to study substrate effect on pillar formation, with etch conducted at various coil RF power and platen bias. Tests were also performed using only a sapphire carrier wafer at various coil RF power to observe the effect of coil RF power on pillar formation. In all cases, samples were sputter cleaned prior to etch to remove residue and grind damage left on the SiC surface.

EFFECT OF RF POWER ON ETCH RATE, SIC TO GAN ETCH SELECTIVITY, AND PILLAR FORMATION

Within coil power range from 1500 W to 2500 W and platen power range from 150 W to 300 W, there is a relatively weak SiC etch rate dependence on coil RF power and much stronger dependence on platen RF power, see Figure 1. This result indicates that within the tested coil power range, the density of ion radicals created by RF plasma remains about constant. However, increased bias (platen power) draws more of the ion species onto the surface. Therefore etch rate is relatively constant vs. coil power but increases with platen power.

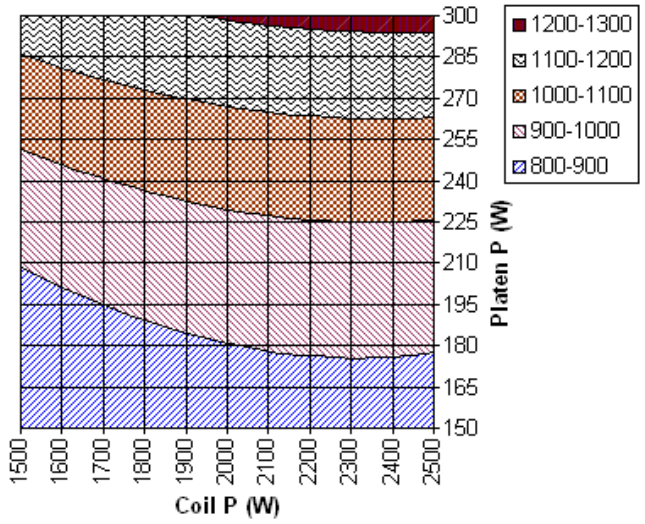

Fig 1 Contour plot of SiC etch rate vs. coil RF power and platen RF power.

The relatively weak dependence of SiC etch rate on coil RF power remains to be the case even when the coil RF power is reduced to <1200 W using patterned test samples. However, reducing coil RF power to these levels resulted severe pillar formation. Figure 2 compares the vias etched at (a) low coil RF power; and (b) high coil RF power. Pillars shown in Figure 2(a) at low coil RF power are typical and exist in nearly every via.

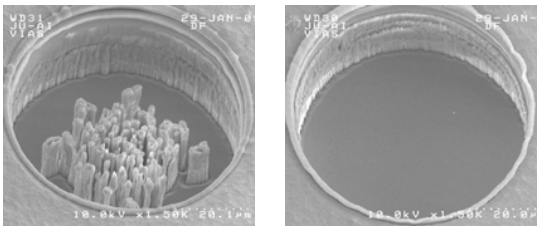

Fig 2 Typical SEM image of via etched at (a) low coil power; and (b) at high coil power.

At increased coil RF power condition, the systematic pillar formation disappeared, leaving some isolated pillars in some vias. Isolated pillar formation in some vias was likely due to the surface not being sufficiently clean prior to reactive ion etch. Whereas systematic pillar formation at low coil power is likely due to the process condition prone to pillar formation, not due to the sample surface condition. It is conceivable that at low coil RF power, the density of certain reactive ion species is somewhat reduced.

While SiC etch rate increased with increasing platen RF power, SiC to GaN etch selectivity is reduced with platen RF power. On the other hand, although SiC etch rate is relatively insensitive to coil RF power, SiC to GaN etch selectivity increased with increasing coil RF power. This is shown in Figure 3.

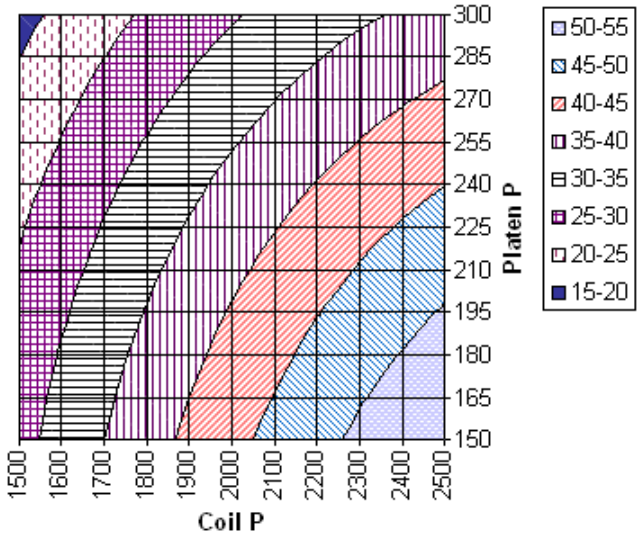

Fig 3 Counter plot of SiC to GaN etch selectivity vs coil and platen RF power.

Even at 1500 W coil RF power, SiC to GaN etch selectivity close to 25 was obtained at low platen RF power (<220 W). This SiC to GaN selectivity is more than sufficient. At higher platen RF power (e.g., 300 W), coil RF power needs to be increased slightly (e.g., to 1800 W) to maintain the same etch selectivity. There is not much practical benefit to further increase coil RF power just for the benefit of increased etch selectivity or SiC etch rate. We have observed two instances when ceramic tooling used to isolate the coil in the small upper part of the chamber failed due to the combination of mechanical and thermal stress. Thus, coil RF power was reduced to reduce thermal stress on the ceramic coil isolator. It is noted that SiC to Ni etch selectivity greater than 50 has been observed in all of the tested RF power range.

EFFECT OF SUBSTRATE ON PILLAR FORMATION

We have also observed gross pillar formation similar to what is shown in Figure 2(a), but under higher coil power. This usually happens when the process chamber is opened to air for wet clean. Gross pillar formation also occurred after the chamber is exposed to Cl_2 and BCl_3. Such gross pillar formation never occurred during process qualification using Ni plated silicon as carrier substrate wafer. It was suspected that carrier substrate had an effect on pillar formation. Therefore a test was performed to compare three different substrates: Ni plated Si, Ni plated sapphire, and Ni plated glass substrates. No gross pillar formation occurred when using Si carrier substrate, intermittent pillar formation was observed using sapphire substrate, and repeated pillar formation was observed when using glass substrate after the chamber was open to air or exposed to Cl_2 and BCl_3.

It is believed that sample temperature is also an important factor affecting pillar formation. Among the three carrier substrates, silicon has the highest thermal conductivity while glass has the lowest. When using temperature "dots" to monitor sample temperature, we observed that sample temperature was ~110C using glass carrier substrate, ~ 80C using silicon or sapphire carrier substrate. For this reason, we believe lowering the sample temperature will reduce gross pillar formation. Lower sample temperature can be achieved by lowering platen temperature. Lowering coil RF power can also reduce sample temperature. However, even at reduced coil RF power, sometimes gross pillar formation still occurs after chamber is exposed to Cl_2 and BCl_3 chemistry using sapphire substrate. Further more, lowering coil RF power too much can by itself result gross pillar formation as shown in figure 2.

METHODS TO REDUCE PILLAR FORMATION

We found that properly season the chamber (subject the chamber to oxygen and SF_6 plasma) can generally help to reduce gross pillar formation when using sapphire or even glass carrier substrates. But sometimes seasoning alone was not sufficient to completely avoid gross pillar formation. This was especially the case when the chamber was open to air and subjected to wet clean. Without further optimizing process condition, one effective way to eliminate such gross pillar formation was to replace chamber hardware.

By properly adjusting pre-etch sputter clean and main etch conditions, gross pillar formation can be totally avoided. Plasma instability that was sometimes associated with gross pillar formation was also observed to disappear completely. The proposed mechanism is that the pre-etch sputter clean, i.e. "breakthrough step", generates a significant amount of Ni that deposits onto the chamber walls. Minimizing Ni sputter deposition can reduce the likelihood of gross pillar formation. This mechanism also partially explains the substrate effect mentioned above. Using glass substrate, the sample temperature is higher than using Si or sapphire substrate. More Ni is sputtered away from Ni hard mask at higher sample temperature. Thus more Ni will be back sputtered onto sample surface, creating more micro-masking and more chance of gross pillar formation using glass substrate.

CONCLUSION

Within a large range of RF power, SiC etch rate was relatively insensitive to the coil power but increases with platen RF power. SiC to GaN etch selectivity increases with coil RF power but decreases with platen power. In practice, SiC to GaN etch selectivity is adequate to stop SiC etch process on GaN surface at relatively low coil RF power. Reducing coil RF power generally reduces the thermal stress on equipment parts and prolongs their lifetime. However, overly reducing the coil RF power can also lead to gross pillar formation during SiC etch. It is thus a balance between avoiding gross pillar formation and extending equipment lifetime when select an optimum RF power condition for the SiC etch process. By seasoning process chamber and by properly modifying pre-etch clean and main etch conditions, gross pillar formation can be further avoided.

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ACRONYMS

ICP: Inductively coupled Plasma