Fabrication Process and 110 GHz Measurement Result of MS-to-CPW RF-Via Transition for RF-MEMS Devices Packaging Applications

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Keywords: Packaging, Fabrication, Microstrip, Microelectromechanical device, Millimeter-wave

Abstract

This paper presents the fabrication process of RF-via (0-level) and flip-chip bump (1-level) transitions for applications of packaging MS (microstrip) RF-MEMS devices. The interconnect structure with MS-to-CPW transition between GaAs MEMS substrate and Al_2O_3 motherboard was in-house fabricated. A novel fabrication process for RF-MEMS packaging is in detail. After fabrication, the samples were measured up to 110 GHz using on-wafer probing measurement. From the measured results, the insertion loss of entire interconnect structure is better than -2 dB up to 100 GHz, documenting the feasibility for millimeter-wave RF-MEMS devices packaging applications.

INTRODUCTION

Radio Frequency Micro-Electro-Mechanical System (RF-MEMS) devices have demonstrated great potential for applications at millimeter-wave frequencies because of several advantages such as high signal linearity, low insertion loss, and power saving [1]. To fabricate reliable RF-MEMS devices for commercial applications, the devices have to be packaged in a stable and hermetic environment [2] with small performance decay. In this regard, RF-via interconnect is considered as a promising packaging method for packaging RF-MEMS devices with excellent RF performance and package reliability [3][4].

RF-via transition is one of the promising schemes at 0-level package to serve RF-MEMS devices for wideband interconnect applications [2]; another candidate for the 0-level package is the RF feed-through [3]. Fig.1 (a) shows the illustration of the 0/1-level packaged RF-MEMS devices, where RF-via transition is used at 0-level package and bump transition is used at 1-level package. In this paper, the two-level interconnect structure is evaluated for MS RF-MEMS devices packaging applications. Fig.1 (b) shows the schematic of the passive 0/1-level interconnect structure in this study. The structure was fabricated in-house using optimized fabrication parameters such as dry via-hole etching conditions, electroplating conditions and bonding conditions. The interconnect structure with two levels of packages demonstrated good interconnect performance up to 100 GHz.

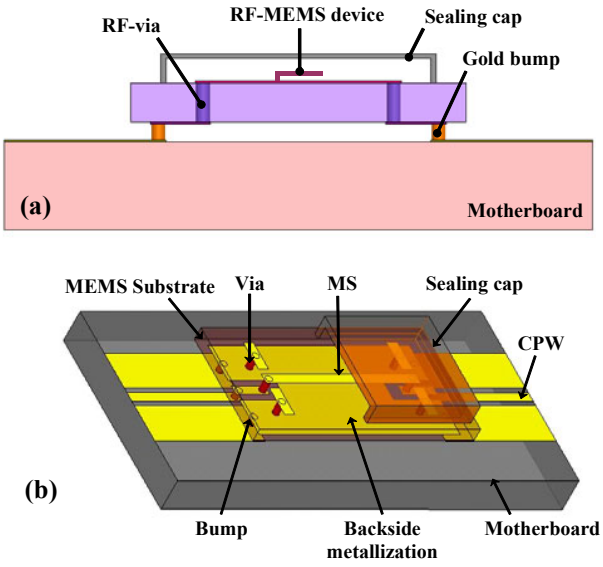

Fig. 1. Proposed (a) 0/1-level package architecture for RF-MEMS devices using RF-via and bump schemes and (b) 0/1-level RF-via interconnect structure of this work.

PACKAGE FABRICATION

The RF-via interconnect structure was fabricated in-house. Fig. 2 shows the process flow of the MS-to-CPW RF-via interconnect structure. The MS transmission lines were first patterned on the front side of the GaAs MEMS substrate by photolithography and electroplating process. The GaAs substrate was then mounted on a sapphire carrier and thinned down to 50~70 μm. RF-via etching was performed by using ICP (inductively coupled plasma) etcher with BCl_3 and Cl_2 gas mixture, where the etching conditions such as the gases mixture ratio, pressure, and etching power were optimized to achieve high etching rate, high etching selectivity, and good etching profiles. The optimized etching parameters are: BCl_3/Cl_2 ratio = 70 sccm/30 sccm, pressure = 10 mTorr, etching coil power = 600 W and etching platen power = 250 W. Fig. 3 shows the cross sectional SEM image of the etched via-hole. The backside metal was patterned on the backside of the MEMS substrate. The fabricated interconnect structure was immersed into the stripping solution to demount the sapphire carrier.

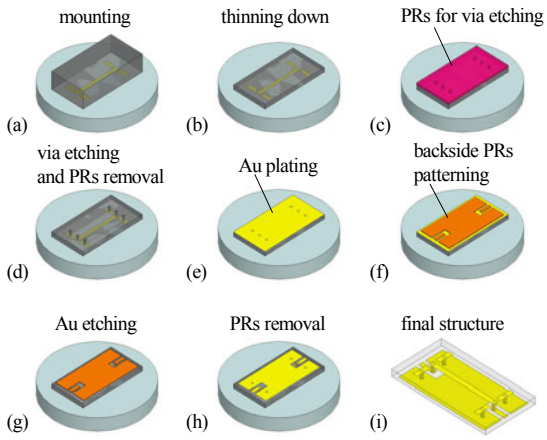

Fig. 2. The process flow of the MS-to-CPW RF-via interconnect structure

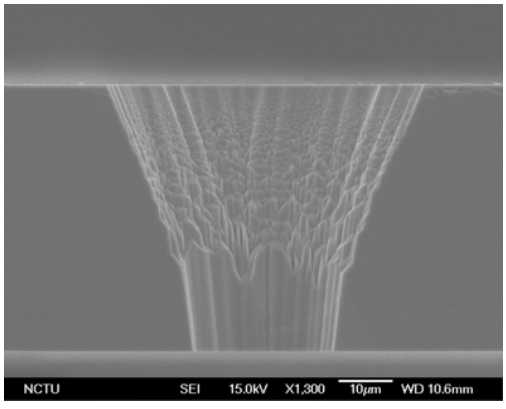

Fig. 3. Cross sectional SEM image of the etched via-hole

The Al_2O_3 motherboard with Au CPW circuits and bumps were fabricated by standard Au bumping process of CSDLab, NCTU [5]. Fig. 4 illustrates the process flow step by step. In the beginning, the metal seed layers Ti and Au were deposited onto the Al_2O_3 motherboard. Then, the thin photoresists were patterned to electroplate the Au CPW transmission line. After the electroplating of the transmission line, the thin photoresists were removed. The thick photoresists were patterned. After that, the pillar bumps were electroplated and the seed layers were removed. The SEM image of the fabricated Al_2O_3 motherboard with Au pillar bumps is shown in Fig.5.

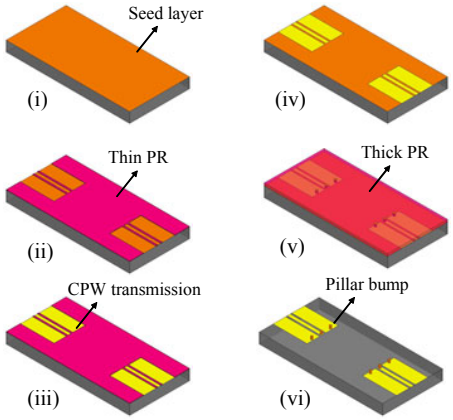

Fig. 4. The process flow of the Al_2O_3 motherboard

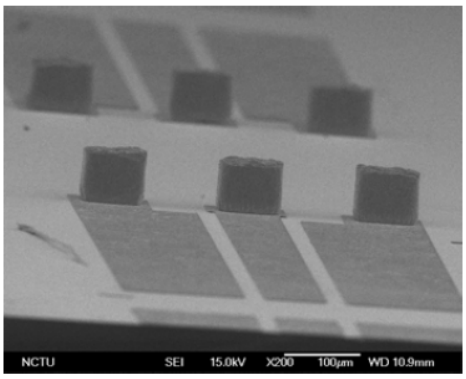

Fig. 5. The SEM image of the fabricated Au bumps on Al_2O_3 motherboard

Finally, the fabricated MEMS substrate with RF-via and the Al_2O_3 motherboard with Au bumps were assembled together by Au-to-Au thermo-compression process and the final interconnect structure was accomplished. The bonding parameters were: bonding force = 120 grams (for 6 bumps), bonding temperature = 300 ^{o}C (for both sides) and bonding hold time = 180 seconds. Fig. 6 shows the SEM image of the fabricated 0/1-level MS-to-CPW RF-via interconnect structure.

S-PARAMETERS RESULTS

The scattering parameters of the fabricated 0/1-level RF-via interconnect structure were characterized up to 110 GHz using the on-wafer probing measurement system with SOLT calibration technique. During the measurements, a 10 mm-thick layer of Rohacell 31 (ε_r=1.04 at 26.5 GHz) was placed between the sample and the metal chuck of the probe station to avoid the backside of the sample from grounding. Fig. 7 shows the measured S-parameters of the back-to-back interconnect structure (including two MS-to-CPW RF-via transitions and two bump transitions). As can been seen, the 0/1-level MS-to-CPW RF-via interconnect structure showed excellent broadband performance up to 60 GHz. The S11 is better than -20 dB and the S21 was better than -0.6 dB from dc to 60 GHz. From 60 to 100 GHz, although the S11 was higher than -10 dB, the S21 was better than -2 dB. These results demonstrate the potential of using this MS-to-CPW RF-via interconnect for MS RF-MEMS devices packaging with applications up to millimeter-wave frequencies.

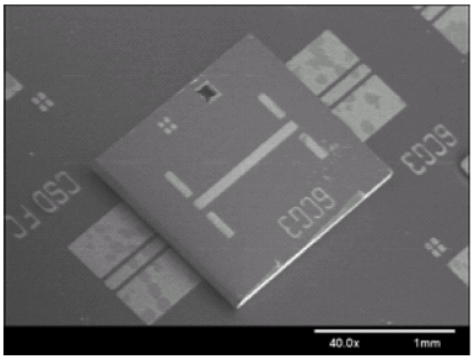

Fig. 6. SEM image of the fabricated back-to-back 0/1-level RF-via interconnect structure.

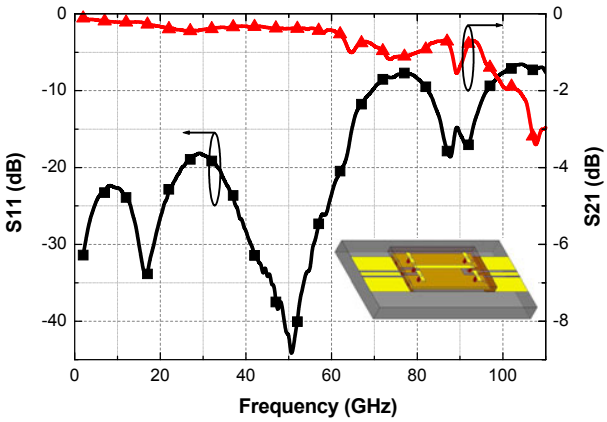

Fig. 7. Measured S-parameters of the back-to-back interconnect structure (including two MS-to-CPW RF-via transitions and two bump transitions).

CONCLUSIONS

A novel fabrication process for 0/1-level RF-via interconnect for MS (microstrip) RF-MEMS devices packaging has been developed and presented. From the dc to 110 GHz measurement, the in-house fabricated MS-to-CPW RF-via two levels package demonstrates excellent performance up to 60 GHz. The S11 is better than -20 dB and the S21 is better than -0.6 dB from dc to 60 GHz. The S21 is better than -2 dB up to 100 GHz, showing promising potential for the structure to be used for millimeter-wave RF-MEMS packaging applications.

ACKNOWLEDGEMENTS

The authors would like to thank C.H. Huang and Y.C. Hu for helping the experimental work. This work was supported by National Science Council and the Ministry of Economic Affairs, Taiwan, under the contracts: NSC 96-2752-E-009-001-PAE and 95-EC-17-A-05-S1-020.

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ACRONYMS

RF-MEMS: Radio Frequency Micro-Electro-Mechanical System
CPW: Coplanar Waveguide
MS: Microstrip